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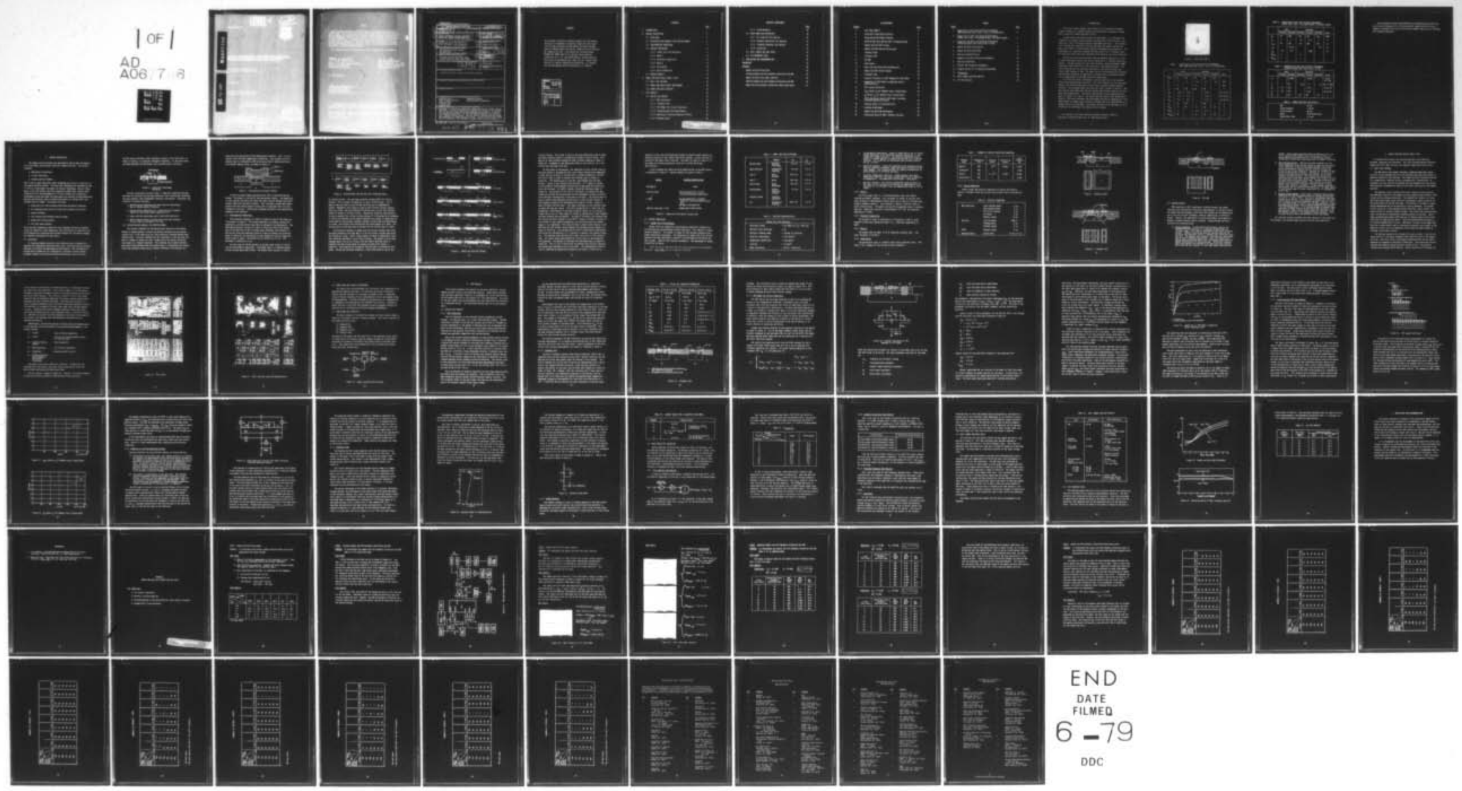

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Development of devices for a monolithic sample and hold on a single chip was undertaken. Process developments were conducted to incorporate a p channel JFET and Schottky diodes into a high speed monolithic process. A test chip was designed and evaluated. The chip included test devices, test circuits and a complete sample-and-hold. The test results indicated that the devices were acceptable for sample and hold circuits. The test results of the sample and hold indicated 7 bit performance at sample rates of up to 50 Msps.

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# FOREWORD

This program to develop a bipolar process with the devices necessary to implement a monolithic sample and hold amplifier has been performed by TRW Defense and Space Systems Group in Redondo Beach, California, under Air Force Contract No. F33615-77-C-1155. The project was initiated under Project No. 6096, Task 10, by the Air Force Avionics Laboratory, M. R. St. John (AFAL/DHE-3), Contract Monitor. The period of performance was 1 May 1977 to 1 August 1978. The work at TRW was planned and directed by L. W. Hobrock and the development effort directed by A. S. Templin.

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# 1. INTRODUCTION

This final report presents the results of a technology development program leading to a bipolar process with the devices necessary to implement a monolithic sample and hold circuit.

Current sample and hold circuits for high speed (1 to 100 Msps) A/D converters are complex costly hybrids utilizing thin film resistors, chip capacitors, JFET transistors and high speed NPN transistors. The introduction of monolithic quantizer circuits[1] has made the sample and hold the major cost factor in A/D converter design, development and production. The development of a monolithic sample and hold circuit will ultimately lead to single-chip monolithic A/D converters with improved cost and reliability.

The key to achieving high speed, high performance operation is a set of high performance devices that can be processed in a standard monolithic process. The key devices are thin film resistors, metal-oxide-metal (MOM) capacitors, NPN transistors, JFET transistors, and Schottky diodes. The first three devices are currently available in the oxide aligned transistor (OAT) process at TRW. The major task of this program was to develop the processes necessary to fabricate a p-channel JFET and Schottky diodes with no degradation to the NPN transistor performance.

To verify the device performance, a device and circuit test pattern (SHD-1) was developed and evaluated. This chip contains not only the basic devices, but also includes test circuits and a complete sample-and-hold function. The packaged sample and hold test chip is shown in Figure 1. The test results have shown that the new process does produce a device set that meets the program goals. The device characteristics are compared to the goals in Tables 1, 2, and 3. The sample and hold results are summarized in Table 4. This data indicates that the sample and hold is adequate for 7 bit applications at sample rates as high as 50 Msps and 9 bit applications at a sample rate of up to 20 Msps. The sample and hold can be extended to 10 to 12 bits at 10 to 20 Msps with modest circuit changes.

1. L.W. Hobrock, "Low Power Radiation Hardened Analog-to Digital Converter," AFAL-TR-75-204, Vol. II, TRW Systems Group.

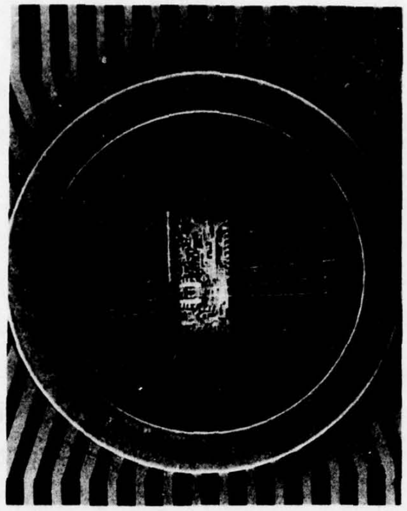


Figure 1. Test Chip (SHD-1)

TABLE 1. COMPARISON OF GOALS AND ACHIEVED PERFORMANCE
(NPN TRANSISTOR, UNIT SIZE = 4 μm x 12 μm EMITTERS)

| | Goal | | Achieved | | | Units |
|---|---|---|---|---|---|---|
| | Minimum | Maximum | Minimum | Typical | Maximum | |
| Beta | 80 | 150 | 50 | 100 | 200 | - |
| $F_t$ | 3 | 5 | 5.0 | 5.5 | 6.0 | GHz |
| $F_\alpha$ | 8 | | 8 | 9 | | GHz |
| $r_b'$ | 150 | 300 | 200 | 300 | | Ω |
| $C_{be}$ | 0.07 | 0.14 | | 0.09 | | pf at 0V |
| $C_{bc}$ | 0.1 | 0.2 | | 0.18 | | pf at 0V |
| $C_{cs}$ | 0.1 | 0.2 | | 0.12 | | pf at 3V |
| $r_c'$ | 75 | 150 | | 100 | | Ω |
| $BV_{ce}$ | 8 | 15 | 8 | 10 | 13 | V |
| $BV_{be}$ | 3 | | 5.0 | 5.5 | | V |
| $BV_{cb0}$ | 20 | | 15 | 20 | 25 | V |

TABLE 2. COMPARISON OF GOALS AND ACHIEVED PERFORMANCE (PJFET, UNIT SIZE = 12 μm GATE WIDTH, 4 μm GATE LENGTH)

| | Goal | | Achieved | | | Units |
|---|---|---|---|---|---|---|
| | Minimum | Maximum | Minimum | Typical | Maximum | |
| $G_m$ | 40 | 300 | 100 | 120 | 150 | μMHO |
| $V_p$ | 1 | 2 | 0.7 | 1.5 | 5 | V |
| $I_{dss}$ | 70 | 430 | 20 | 100 | 400 | μA |
| $I_{gc}$ | | 10 μA | | | 0.8 | μA |
| $C_{gc}$ | 0.1 | 0.2 | | 0.08 | | pf |
| $BV_{g-s}$ | 7 | | 7 | | | |
| $BV_{g-d}$ | 7 | | 7 | | | |

TABLE 3. COMPARISON OF GOALS AND ACHIEVED PERFORMANCE (SCHOTTKY DIODE, UNIT SIZE 20 μm x 24 μm)

| | Goal | | Achieved | | | Units |
|---|---|---|---|---|---|---|
| | Minimum | Maximum | Minimum | Typical | Maximum | |
| $V_f$ | | 0.460V | | 0.600 | | Volts at 1 mA |
| $I_r$ | | 10 | 0.45 | 1.1 | 1.7 | na at $100^oC$ |
| $C_p$ | 0.1 | 0.2 | | 0.12 | | pf at 0V |
| $C_s$ | 0.1 | 0.2 | | 0.13 | | pf at 3V |
| $R_s$ | | 20 | 22 | 40 | 70 | Ω |

TABLE 4. SAMPLE AND HOLD TEST RESULTS

| | |
|---|---|
| SNR | 52 dB |
| Second Harmonic | <-60 dB |
| Third Harmonic | -53 dB |
| Droop | 0.25 mV/120 nsec |
| Acquisition Time | 11 nsec |

This program has proven the feasibility of producing the devices and the circuitry necessary for a fully monolithic sample and hold circuit capable of operating at 10 to 12 bits and at sample rates of up to 100 Msps with reduced resolution.

## 2. PROCESS DESCRIPTION

The sample and hold process was developed by TRW to meet the demands of a high speed, high accuracy monolithic sample and hold. The process produces:

- NPN bipolar transistors
- P-JFET transistors
- Schottky barrier diodes.

TRW's oxide aligned transistor (OAT) technology was used as a baseline for the sample and hold process. The basic OAT technology was developed by TRW in 1971 as a high speed, low power LSI bipolar technology. Recent refinements in the OAT process have been supported by AFML under contract AFML-IR-503-5(11) for the development of a 10 bit, 10 MHz A to D converter. Improvements which have been realized under this contract include additional masking and diffusion steps to extend the process to include JFET's and Schottky barrier diodes. The process utilizes:

- Oxide wells for self-aligning diffusions and device isolation
- Ion implanted base that also serves the p-channel for the FET
- Arsenic emitters
- PtSi contacts and Schottky barrier diodes
- Cermet thin film resistors
- Two level metallization.

Since the small geometries needed for high frequency devices are opposed to the LSI complexity level objectives, the utilization of oxide wells for self-aligning and a polycrystaline arsenic emitter for low device leakage are important techniques for high yield.

### 2.1 OXIDE WELL

In industry standard practice, each diffusion step is masked by a separate and independent photoresist-etch step. Each mask must be aligned precisely to maintain minimum geometry construction. The limitations on minimum device dimensions are consequently a function of best routine alignment capability and worst-case mask distortions, such as run-out.

The OAT process minimizes these problems by using a thick oxide well, as shown in Figure 2, to prealign subsequent diffusions. In the case shown, one mask prealigns two diffusions, plus provides device isolation.

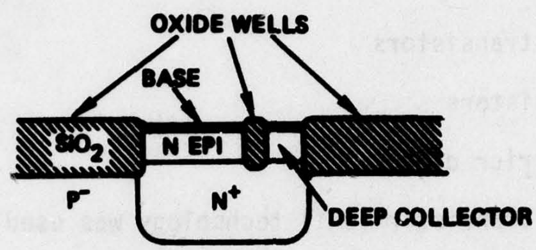



Figure 2. Oxide Well Prealigned Diffusion

Two well structures are used in OAT: a deep well prealigns the deep collector N+ diffusion and the base diffusion; and a shallow well prealigns the base contacts, base enhancement diffusion, and emitter. Therefore, the oxide well structure provides:

- Smaller device dimensions and lower junction capacitance due to limited lateral diffusion
- Smaller device dimensions for a given mask and alignment capability (providing higher complexity LSI)
- Lower junction capacitance due to the oxide side walls
- Smaller base-collector junction area since base contacts can be placed at the edge of the base.

## 2.2 POLYCRYSTALLINE ARSENIC (PA) EMITTER SOURCE

The industry standard for the emitter-base structure of microwave devices is washed emitter in which the emitter diffusion and the emitter contact occur in the same oxide cut, thus producing a minimum emitter-base junction area. The basic problem with this technique is that the etch dip which is needed to remove the $SiO_2$, formed during the emitter diffusion, also etches in a lateral direction. This enhances the incipient emitter-base short which develops when the contact metal is evaporated and alloyed, since this approach relies only on lateral diffusion of the emitter for

protection and passivation of the emitter-base junction. This, in turn, reduces yield and high temperature reliability. This standard critical process step is eliminated in OAT by using an arsenic doped polycrystalline emitter doping source, as shown in Figure 3.

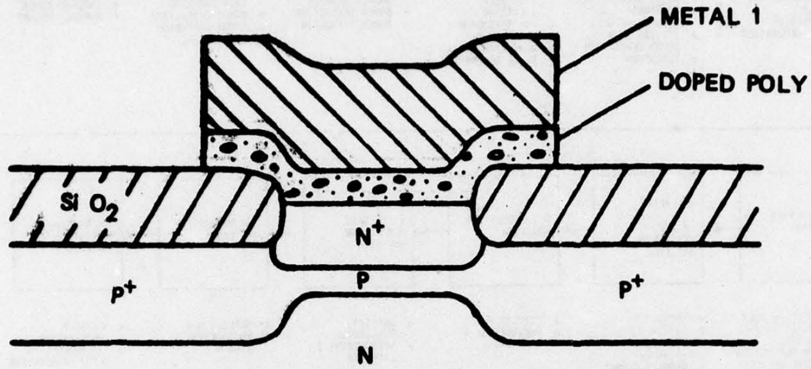



Figure 3. Polycrystalline Arsenic Emitter

A heavily arsenic doped polycrystalline film is deposited and patterned. The arsenic is driven to form the emitter region. The doped poly is then covered with metal and forms the ohmic contact between the active emitter region and the metal contact. Thus, the metal system never makes contact with the single crystal silicon and is separated from it by the thickness of the poly. Emitter-base leakages and shorts are substantially reduced by this approach.

## 2.3 SEMICONDUCTOR PROCESSING

The processing sequence is listed in Figure 4; many of the steps are illustrated in Figure 5. The P-type substrate is oxidized, coated with photoresist, and the buried layer mask is exposed in the photoresist. The developed photoresist serves as a mask to allow the oxide to be etched away in the position of the $N^+$ buried layer diffusion; the diffusion is carried out using the remaining oxide as a mask to produce the structure shown in Figure 5a. The oxide mask is then etched off, and an N-type epitaxial layer is grown. The resistivity is typically 0.4 Ω-cm. The thickness is typically 0.2 μm.

The next step of the OAT process is to grow three layers of insulation on the surface of the wafer. The bottom layer is a thermally grown silicon dioxide about 200 Å thick. The middle layer consists of 1000 Å

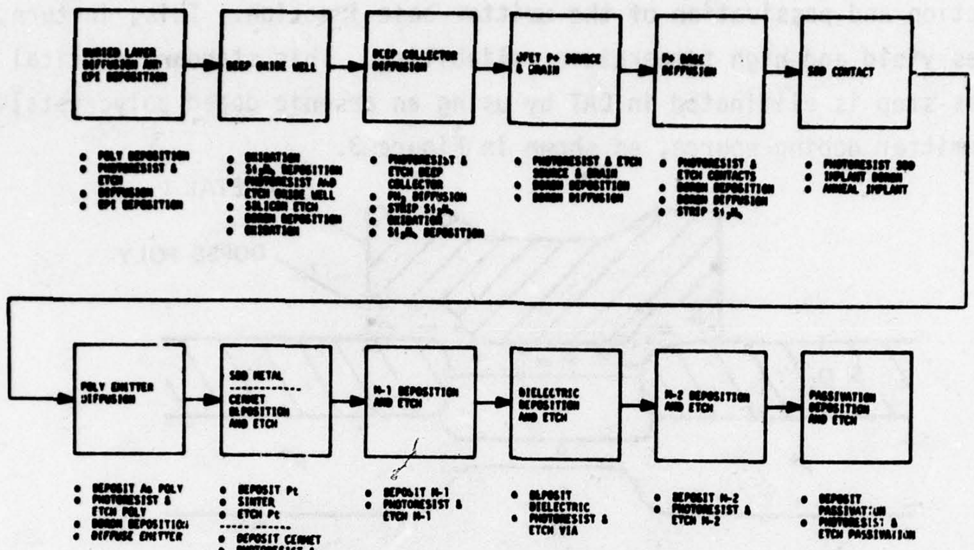



Figure 4. Modified OAT with SBD and JFET 12 Masking Steps

of silicon nitride. The top layer consists of about 500 Å of silicon dioxide. *This is shown in Figure 5b, as just a nitride layer.* Use is made of the fact that silicon nitride and $SiO_2$ can be independently etched. Phosphoric acid, which is used to etch silicon nitride, attacks $SiO_2$ very slowly, and the buffered HF solution used to etch $SiO_2$ exhibits almost no attack on silicon nitride. Photoresist cannot be used directly to etch a pattern into silicon nitride because it is attacked by hot phosphoric acid; but patterns can be etched indirectly by growing or depositing an oxide layer on the nitride, etching a pattern in the oxide with photoresist as a mask, then etching the nitride with the oxide pattern as a mask. The bottom layer of oxide may then be etched with the nitride used as a mask.

The oxide well pattern is etched into the silicon nitride layer with the above procedure; and then about 1.0 μm of silicon is etched away using the nitride as a mask. Next, a small amount of boron is deposited to prevent inversion and about 1 μm of oxide is grown. The growth of this oxide consumes about 0.45 μm of silicon, with the result that the oxide is recessed into the silicon wafer to produce the deep wells shown in Figure 5c. The isolation of one device from the next is provided by this oxide. During the isolation oxidation, a thin oxide forms on top of the

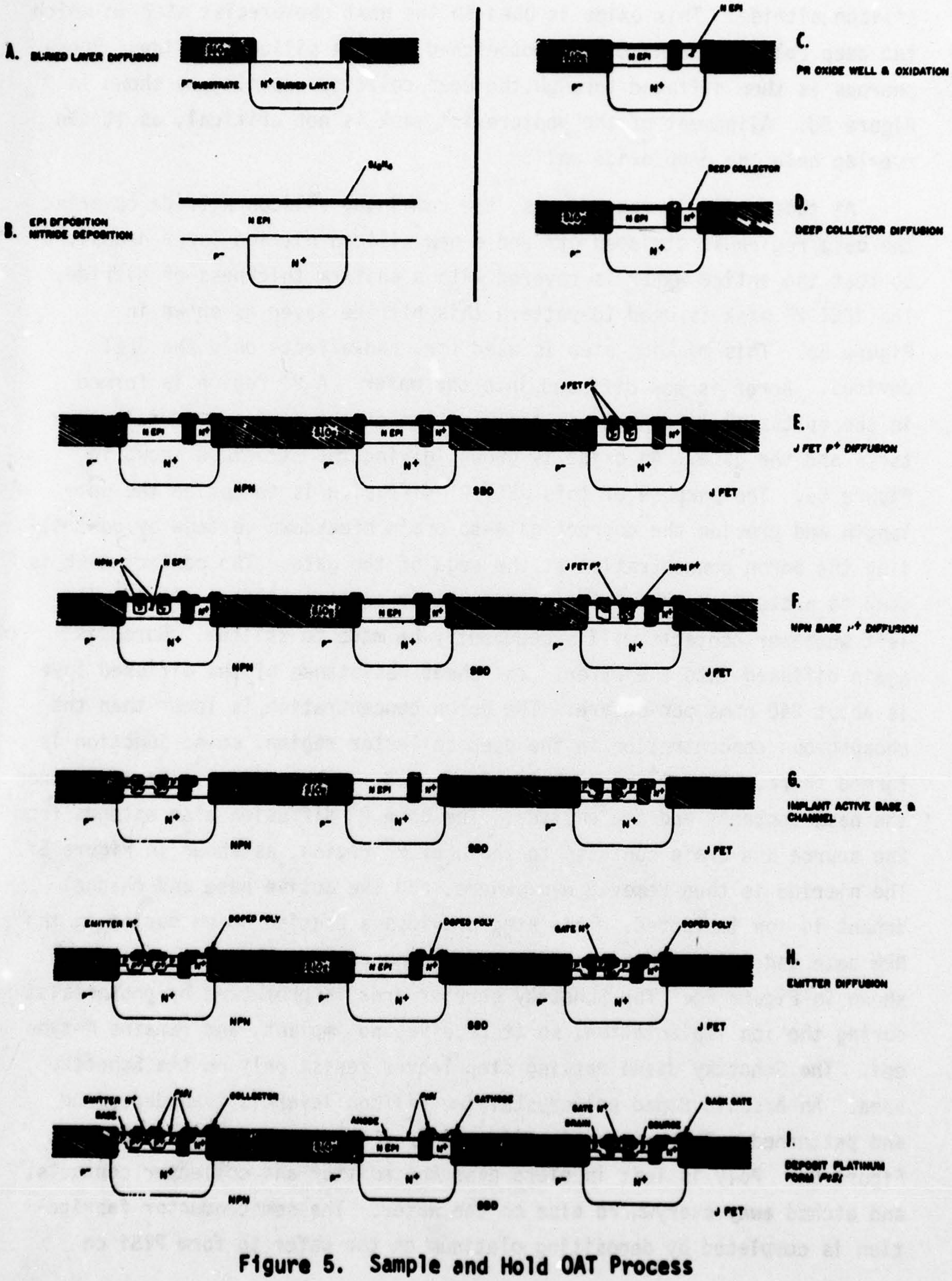



**Figure 5. Sample and Hold OAT Process**

silicon nitride. This oxide is used in the next photoresist step in which the deep collector contact is photoetched through silicon nitride. Phosphorous is then diffused through the deep collector opening as shown in Figure 5d. Alignment of the photoresist mask is not critical, as it can overlap onto the deep oxide well.

At this point in the process, the remaining silicon nitride covering the base region is stripped off and a new silicon nitride layer deposited so that the entire wafer is covered with a uniform thickness of nitride. The JFET $P^+$ mask is used to pattern this nitride layer as shown in Figure 5e. This masking step is used for, and affects only the JFET devices. Boron is now diffused into the wafer. A $P^+$ region is formed in the epitaxial layer between the position of the source and drain contacts and the gate. An oxide is grown, giving the structure shown in Figure 5e. The purpose of this JFET $P^+$ diffusion is to define the gate length and provide the correct gate-to-drain breakdown voltage by controlling the boron concentration at the edge of the gate. The contact mask is used to pattern the remaining nitride layer so that silicon nitride is left wherever contacts will subsequently be made to silicon. Boron is again diffused into the wafer. The sheet resistance of the diffused layer is about 240 ohms per square. The boron concentration is lower than the phosphorous concentration in the deep collector region, so no junction is formed there, but a $P^+$ base region is formed in the epitaxial layer between the base contacts and the emitter. The base $P^+$ diffusion also extends from the source and drain contacts to the JFET $P^+$ region, as shown in Figure 5f. The nitride is then removed everywhere, and the active base and channel dopant is ion implanted. This step provides a precise boron doping in the NPN base and JFET channel active regions and provides contact doping, as shown in Figure 5g. The Schottky barrier area is protected by photoresist during the ion implantation, so it receives no implant, and remains N-type epi. The Schottky diode masking step leaves resist only on the Schottky area. An arsenic doped polycrystalline silicon layer is then deposited and patterned. The emitter is diffused from the doped poly, as shown in Figure 5h. Poly is left in place over the emitter and collector contacts, and etched away everywhere else on the wafer. The semiconductor fabrication is completed by depositing platinum on the wafer to form PtSi on

exposed silicon, thus providing good contact on heavily doped regions and Schottky contacts to the lightly doped N-epi regions. Excess platinum is etched off the wafer after sintering. The wafer as shown in Figure 5i is now ready for surface processing, which will include multilayer metallization.

A chart showing the sample and hold modifications to the OAT process is presented in Figure 6. Junction depths are given in Table 5.

| DEVICE | PROCESS MODIFICATION |
| --- | --- |
| NPN BIPOLAR | NONE |
| SCHOTTKY DIODE | ADD ONE MASKING STEP - TO AVOID IMPLANTING BORON INTO DIODE REGION |
| p-JFET | ADD ONE MASKING STEP - TO PROVIDE SEPARATE P + DIFFUSION UNDER SHALLOW WELL<br>ADD ONE P + DIFFUSION STEP |
| SCHOTTKY DIODE AND p-JFET | COMBINE ABOVE MODIFICATIONS |

Figure 6. Sample and Hold Device Process Work

## 2.4 SURFACE PROCESSING

### 2.4.1 Cermet Thin Film Resistors

Cermet films are prepared by simultaneously depositing chromium and silicon monoxide using separate electron beam guns. This results in stable resistive material. The cermet is etched to form resistor patterns using normal photoresist techniques. The technology of cermet thin film, on-chip resistors has been described at length[1,2] and developed by TRW during the last 5 years. Table 6 lists resistor parameters. The advantages of cermet include the following:

2. Braun and Lood, "Precision Thin Film Cermet Resistors for Integrated Circuits," Proc. IEEE, Vol 54, 1966, pp. 1521-1527.

TABLE 5. SAMPLE AND HOLD DIFFUSIONS

| | Dopant | $R_S$ | $X_J$ |
|---|---|---|---|
| Buried Layer | Antimony from $Sb_2O_3$ | 20 Ω/sq | 3.0 μm |
| Deep Collector | Phosphorous from $PH_3$ | 10 Ω/sq | 3.0 μm |
| JFET $P^+$ | Boron from BN | 400 Ω/sq | 1.2 μm |
| NPN $P^+$ | Boron | 240 Ω/sq | 0.9 μm |
| Active Base | Boron implanted | 700 Ω/sq | 0.3 μm |
| Emitter/Gate | Arsenic from poly silicon | 15 Ω/sq | 0.2 μm |
| Schottky Diode | Platinum sputtered | - | - |
| Epi | Phosphorous from $PH_3$ | 2000 Ω/sq | 2.0 μm |

TABLE 6. RESISTOR CHARACTERISTICS

| Cermet Thin Film Resistors | |
|---|---|
| Resistance range | = 25 -5000 Ω at $R_S$ = 100 Ω/sq |
| Resistor ratio tolerance | ≤ 1% |
| Resistor trimming range | > 10% max to 0.01% min |
| Parasitic capacitance | = 0.02 pF/$mil^2$ |
| Temperature coefficient | = -100 ppm/°C |
| Tracking | = ±3 ppm/°C |
| Sheet resistance | < 100 to > 1000 Ω/sq |

- Low parasitic capacitance. Cermet is deposited on top of thermal oxide; therefore, no pn isolation junction capacitance is associated with cermet resistors. The parasitic substrate capacitance of a cermet resistor is about 0.02 pF/mil$^2$ (for a 100 ohm resistor. $C_S$ = 0.005 pF; an equivalent base diffused resistor has $C_S$ = 0.1 pF).

- Radiation hardness. Since the chromium-silicon monoxide mixture used for cermet is amorphous, gamma and neutron radiation do not cause damage. Also, radiation does not cause the generation of photocurrents as in diffused resistors.

- Excellent temperature stability. Cermet exhibits very good temperature stability, and does not have mobility as a function of temperature. The temperature coefficient = -100 ppm/°C.

- Resistor tracking. The tracking coefficient (the deviation in the ratio of two resistors as a function of temperature) is of the order of 1 to 10 ppm/°C over the temperature range of -55 to +125°C.

### 2.4.2 Metal-1

The first metal layer is a titanium-aluminum layer with 1500 Å titanium and 5000 Å aluminum. This thickness is chosen to provide sufficient coverage of semiconductor device steps and to keep at a minimum step heights created by metal-1. The titanium is used as a barrier layer to avoid sintering pits. The metals are serially evaporated using an electron beam gun. Deposition pressure is approximately $10^{-6}$ torr and substrate temperature is 300°C.

### 2.4.3 Dielectric Deposition

The dielectric layer is deposited to a thickness of 7000 Å, using standard silane vapor deposition techniques. Substrate temperature is 400°C.

### 2.4.4 Metal-2

The second level of metal is an RF sputtered aluminum layer. The layer thickness is 12,000 Å.

### 2.4.5 Passivation

The passivation layer is a 3000 Å silane vapor deposited layer. See Table 7 for a summary of the surface process parameters.

TABLE 7. SUMMARY OF SURFACE PROCESSING PARAMETERS

| Process Step | Temperature (ºC) | Pressure (torr) | Resistivity (Ω/sq) | Layer Thickness (Å) |
|---|---|---|---|---|
| Metal-1 | 300 | $10^{-8}$ | ~0.045 | 6,500 |
| Dielectric | 400 | - | - | 7,000 |
| Metal-2 | 200 | $6 \times 10^{-3}$ | ~0.035 | 12,000 |
| Passivation | 400 | - | - | 3,000 |

### 2.4.6 Device Dimensions

Table 8 shows the physical dimensions of typical OAT devices. Figures 7 through 9 show the top and cross-section view of each device type.

TABLE 8. PHYSICAL DIMENSIONS

| | | |
|---|---|---|
| NPN Transistor | Final Emitter Width | 2 μm |
| | Base Contact Width | 4 μm |
| | M-1 to M-1 Spacing | 2 μm |
| | M-1 Width | 8 μm |
| | Emitter Length | 12 μm |
| Resistor | Film Thickness | 1000 Å |
| | Minimum Width | 8 μm |
| | Minimum Length | 8 μm |
| PJFET | Channel Length | 2 μm |
| Schottky Diode | Active Area | 17 μm x 21 μm |

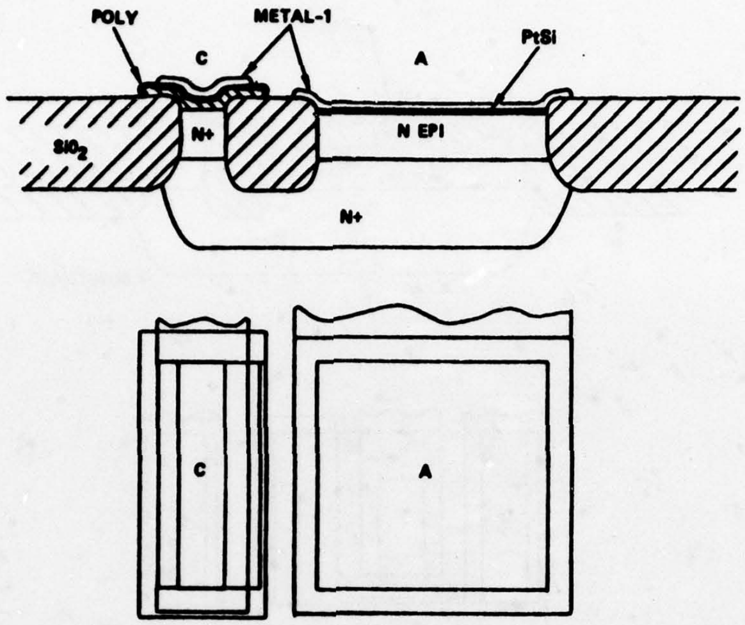



Figure 7. Schottky Diode

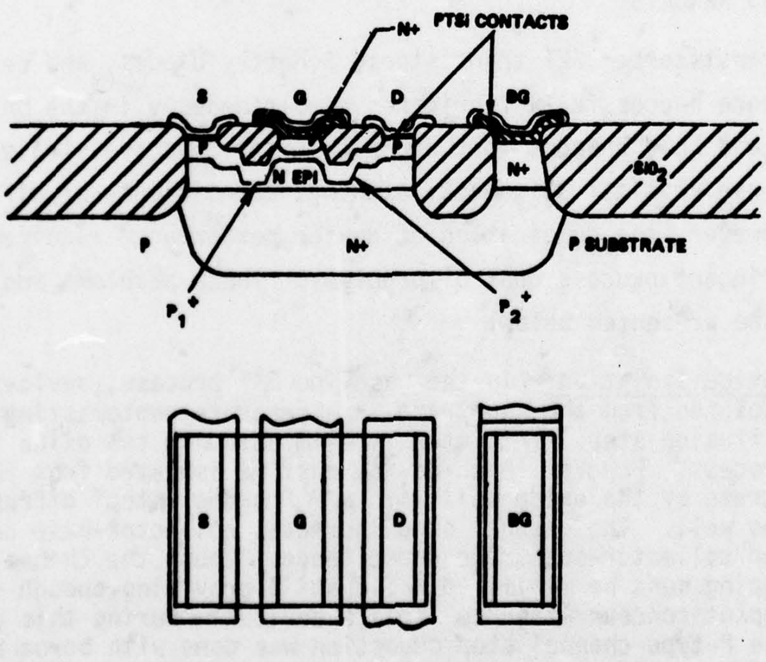



Figure 8. P-Channel JFET

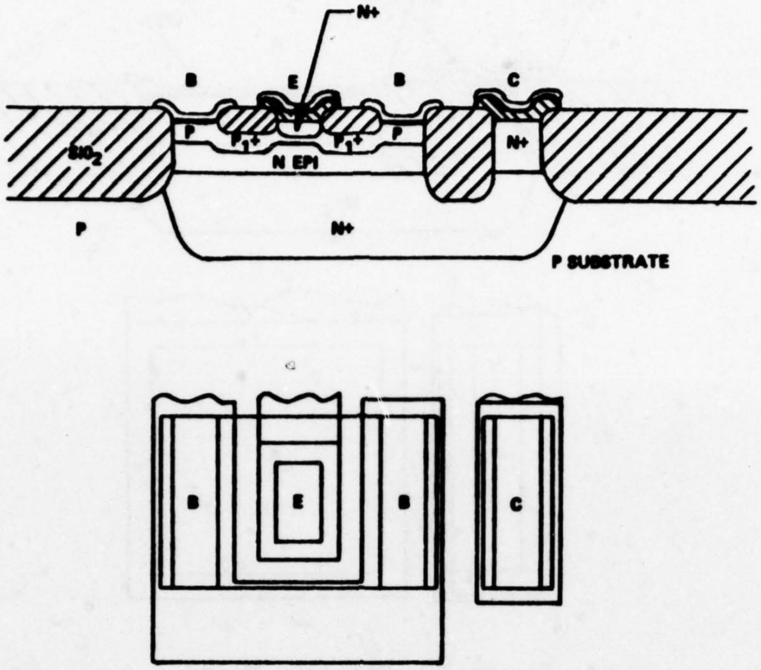



Figure 9. OAT NPN

## 2.5 PROCESS RESULTS

NPN transistors, JFET transistors, Schottky diodes, and cermet resistors were successfully fabricated simultaneously in the OAT process. The sample and hold changes to the basic OAT process are straightforward and do not use critical alignment, etching, depositions, or diffusion depths. However, the combination of device performance requirements do present stringent process control problems. These problems and their solutions are presented below.

1) Device Isolation. In the baseline OAT process, devices are isolated from the substrate in a separate photomasking and diffusion step. This step is eliminated in the oxide isolation process. However, each device must be isolated from the substrate by the oxide well with a P "channel stop" diffusion under the well. The channel stop increases collector-base capacitance and collector-substrate capacitance. Thus, the channel stop doping must be minimized while still providing enough depth and dopant concentration to isolate devices. During this program, the P-type channel stop depostion was done with boron nitride, which provides poor control for the light dopant concentration

needed. Future sample and hold oxide isolated parts will use an ion implant boron channel stop so that exact control of dopant depth and concentration will be maintained, without increasing collector-base capacitance due to sidewall diffusion.

2) JFET Pinchoff Control. NPN beta and JFET pinchoff are both highly dependent on the emitter diffusion depth and base width. It was found that producing reasonable NPN beta (50 to 200) while simultaneously controlling JFET pinchoff voltage was difficult due to the diffusion of the base (an increase in base width) during emitter diffusion. Effectively, an increase in emitter diffusion would increase beta quickly, while barely lowering the JFET pinchoff. This problem was corrected by decreasing the active base implant energy from 70 keV to 60 keV, while maintaining the same total dose. The base width was thus narrower, with a steeper profile. This results in pinchoff being a fast function of emitter diffusion (as well as beta being a fast function, as normal). In this manner, both beta and pinchoff can be controlled satisfactorily. An added benefit of the narrower base is faster transistors, as $f_T$ increased to about 6 GHz.

3) Schottky Diode Leakage. Early tests on Schottky diodes approximately 20 μm x 20 μm indicated that low leakage was obtained (0.1 nA at -1 volts, 100°C). The first lots produced had high leakage (5 to 100 nA). This increase in leakage was correlated with a change in platinum sputtering machines. Due to a lack of a platinum target in the OAT lab, and down equipment in other Microelectronics Center Labs, platinum sputtering was obtained from TRW Semiconductors. This platinum seemed to produce leaky junctions, probably because of gold which was sputtered in the same machine. When a new platinum target was installed in the OAT process laboratory, low leakage was again produced. Care is being taken to avoid contamination of this new target.

All the major process problems have been resolved in the sample and hold process, and working sample and hold circuits have been built.

# 3. SAMPLE AND HOLD DEVICE (SHD-1) CHIP

To evaluate the process and resulting devices a test chip was designed, processed, and evaluated. This chip included devices (Schottky diodes and FET's) test circuits, and complete sample and hold circuits.

## 3.1 SHD-1 TEST PATTERN

The SHD device test pattern includes a complete monolithic sample and hold circuit designed and laid out with many test pads and options to maximize flexibility and learning. The sample and hold circuitry consists of a preamplifier, sampling circuit, postamplifier, strobe buffer, dc reference, and two circuits associated with the postamplifier that employ PJFET devices to enhance the acquisition-to-hold time ratio of the sample and hold.

The sampling circuit performs the actual sample and hold function. The remaining circuits in the sample and hold provide level shifting, interfacing, and dc reference functions. The preamplifier serves to dc level shift the analog input signal and also incorporates a gate to switch off the analog input during the hold mode. This gating is intended to reduce analog feedthrough and can be optionally used or defeated. The postamplifier serves as a high impedance buffer amplifier, level shifter, and output driver for the held signal voltage. The circuit has three possible input configurations selectable by bonding options on the chip. Two of these configurations employ PJFET devices to improve acquisition-to-hold time ratio by reducing hold droop. The third configuration provides an all bipolar postamplifier circuit. Additional circuits in the sample and hold are a strobe buffer used to interface an external clock signal to the sampling circuit, and a dc reference circuit which provides various dc voltages to the other circuits.

The SHD test pattern also includes five test circuits. The first of these circuits is the basic wideband linear amplifier used in the sample and hold. From this circuit, performance characteristics can be readily measured and compared to analytical predictions. The second test circuit contains two negative and one positive current mirror. The positive current mirror employs PJFET devices. These circuits are of interest for

a wide range of applications including amplifiers, dc reference circuits, and sample and hold amplifiers. Test circuit number 3 is a high speed, extremely high output impedance current switch made possible by the availability of PJFET devices. This circuit is useful in 12 to 16 bit high speed A/D and D/A converters where the all bipolar current switch output impedance can cause linearity problems. The fourth test circuit is a bipolar bandgap reference circuit and PJFET operational amplifier circuit. The amplifier is projected to be much lower power than previous bipolar circuits. Combining this with a bandgap reference circuit will allow application oriented testing of the combined circuit. The fifth circuit is a 1200 MHz all bipolar flip-flop designed to test the circuit speed of the process, and guarantee that the additional processing has not degraded performance.

Additionally, the SHD test pattern includes single and matched pairs of test devices, with Kelvin pads to allow accurate measurements. The devices include:

| | |
|---|---|
| • P-JFET | Seven different geometries |
| • P-JFET | Four sets of interdigitated devices to study matching |
| • Schottky Barrier Diodes | Three geometries |
| • NPN Transistors | Six different geometries |
| • Capacitors | Junction and M-1 to M-2 |
| • DC Resistance and High Frequency Calibration Structures | |

The overall chip size is 204 mils x 235 mils. Scribe lines are included within the chip so that test circuits may be cut out of the wafer without destroying the area around them.

The chip layout is shown in Figure 10. Figure 11 is a block diagram of the chip with the location of each section of test circuitry.

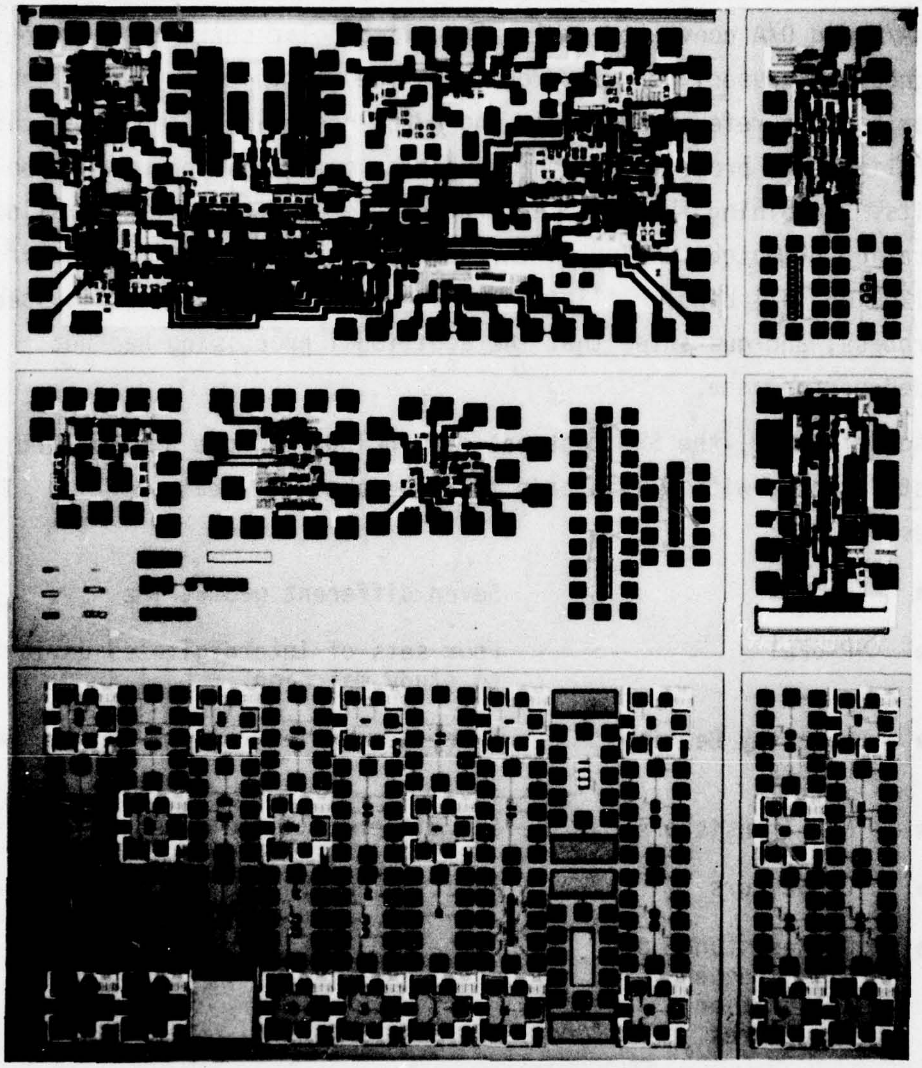


Figure 10. Chip Layout

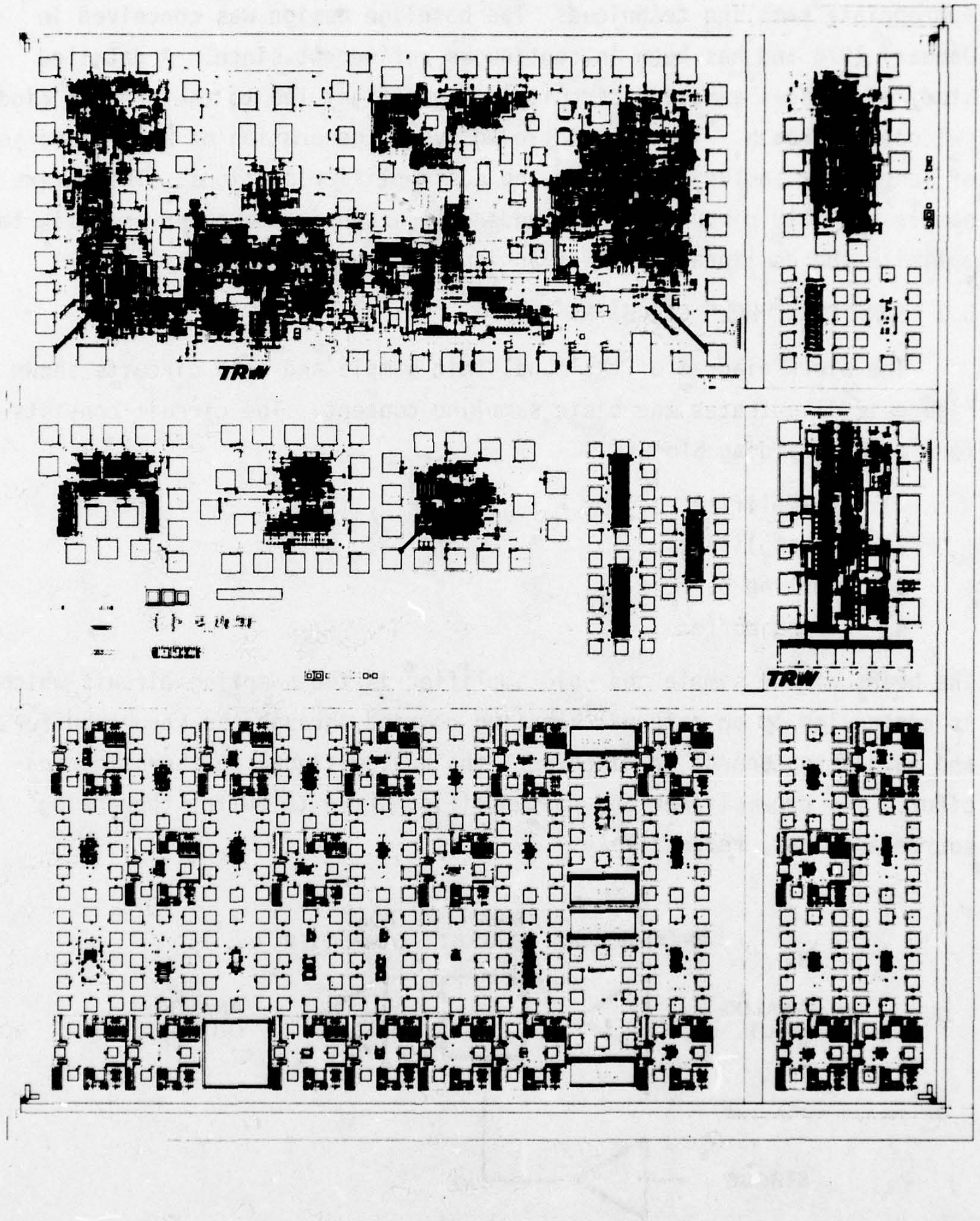



**Figure 11. SHD-1 and Test Array DIE Configuration**

## 3.2 SAMPLE AND HOLD CIRCUIT DEVELOPMENT

The sample and hold development was initiated by the conception of an appropriate sampling technique. The baseline design was conceived in January 1976 and has been in continuous refinement since. A detailed study of various sampling circuit configurations led to the present diode-switched approach. This was followed by the generation of a complete set of schematics including the pre and postamplifier sections. The entire sample and hold circuit has now undergone extensive computer analysis to optimize the dc linearity and transient response performance.

## 3.3 SAMPLE AND HOLD CIRCUITRY

The block diagram of the monolithic sample and hold circuits shown in Figure 12 illustrates the basic sampling concept. The circuit consists of four major building blocks:

1) Preamplifier
2) Postamplifier
3) Sampling circuit
4) Strobe buffer.

The heart of the sample and hold amplifier is the sampling circuit which is controlled by an external sampling command through the strobe buffer, and serves to connect or disconnect the analog signal to the hold capacitor. The preamplifier and postamplifier serve to buffer the analog source and load, respectively.

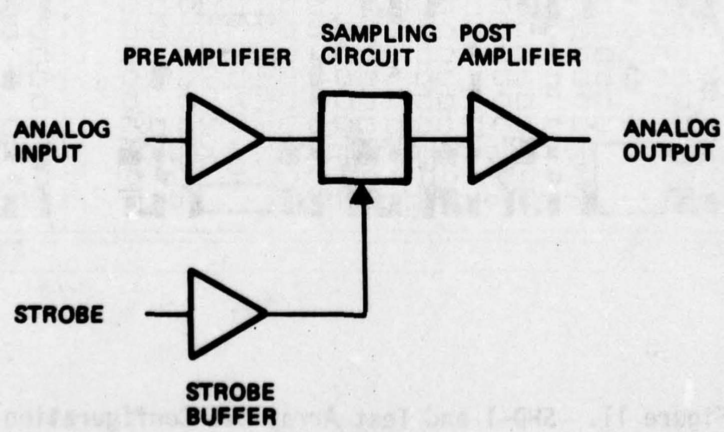



Figure 12. Sample and Hold Block Diagram

# 4. TEST RESULTS

This section presents the results for the basic amplifier, bipolar sample and hold circuit, and individual devices. These tests indicated that the basic amplifier linearity is acceptable for 10 bit applications, and the sample and hold is only useful for 7 bit applications. The cause of the poor sample and hold performance has been identified and corrected in a subsequent design. The individual devices meet all of the program goals.

## 4.1 DEVICE TEST RESULTS

### 4.1.1 NPN Transistors

The NPN transistor is the principal device produced by the OAT process. For the most part, it is well characterized already. The NPN transistors included in the SHD test pattern were primarily intended to provide information on the degree of matching that can be obtained from pairs of OAT transistors, and also to verify that process modifications required for the junction field-effect transistors and Schottky barrier diodes were genuinely compatible with the NPN devices.

One of the crucial design parameters in high accuracy analog circuits is the degree to which transistor base-emitter voltage ($V_{be}$) is matched. A typical OAT device intended to have good high frequency response has an emitter stripe width of 3 or 4 μm on the mask, which results in an active emitter width of 2 to 3 μm. A small absolute variation in emitter width may then be a relatively large percentage variation in emitter area, and thus in $V_{be}$. A series of pairs of devices with constant nominal emitter area and various emitter geometries was fabricated to determine the relationship between emitter geometry and device matching. The emitter sizes of the transistors for which detailed matching measurements were made included three stripes each 3 μm x 12 μm, two stripes each 4 μm x 12 μm, and one stripe 6.5 μm x 12 μm.

The 3 μm devices are normally used only for very high speed circuits, and should have the poorest $V_{be}$ matching. The 4 μm emitter width has been standardly used on analog circuits and most digital circuits. The 6.5 μm emitter width is the next larger size that can be conveniently used in the present computer-aided layout system.

$V_{be}$ was measured with the transistors operating at a specified collector emitter voltage (usually 1 volt) and at various emitter currents from 0.2 to 6 mA; most of the $V_{be}$ matching measurements were done at 0.6 mA. At this current the $V_{be}$ mismatch of a pair, averaged over about 50 pairs of each kind of transistor, was 1.0 mV for the 3 μm emitter width, 0.50 mV for the 4 μm emitter width, and 0.38 mV for the 6.5 μm emitter widths.

Measurements were made of the change with temperature of the difference in $V_{be}$ of a transistor pair with both transistors operating at the same current, and with the currents adjusted for zero offset at 25°C. Pairs of 6.5 μm transistors from the SHD last pattern were compared with transistor pairs with a single 4 x 12 μm emitter stripe, taken from another OAT circuit. The change in differential $V_{be}$ for the 6.5 μm device was typically about 0.1 mV over the range -25 to +100°C for either equal currents or with currents trimmed for minimum offset. The differential $V_{be}$ of the 4 μm pairs varied about 0.25 to 0.5 mV under similar conditions. The significance of these data would be greater if all the transistor pairs had been processed together, but it strongly favors the wider emitter stripe for high accuracy analog circuitry.

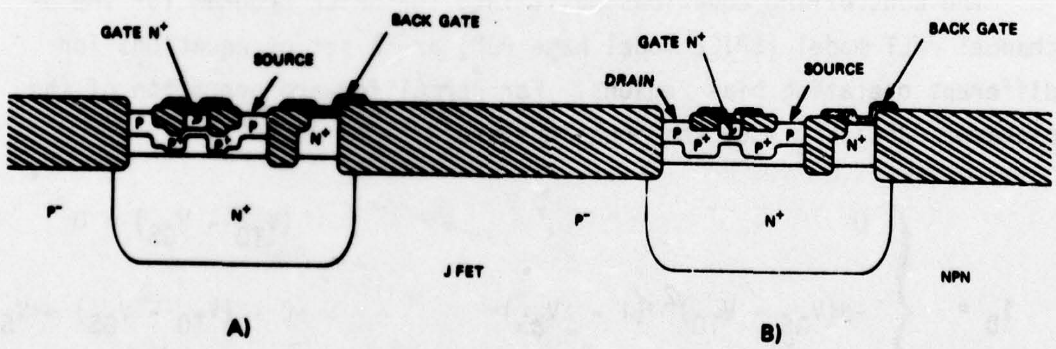
The typical parameters for OAT transistors are fairly well known from previous measurements, so no complete characterizations of the transistors from this particular test chip were done. Typical parameters of OAT transistors from previous measurements are shown for reference in Table 9.

#### 4.1.2 P-Channel JFET

The basic p-channel junction field effect transistor (JFET) that is compatible with the OAT process utilizes the $n^+$ emitter diffusion for the gate and the active base region under the emitter as the channel. The initial feasibility of this sort of device was demonstrated with a variation of the standard NPN OAT transistor, using one base contact as a source, the emitter as the gate, and the other base contact as a drain as shown in Figure 13b. However, with this structure the $p^+$ base used for the npn transistor lies immediately adjacent to the emitter, and the doping level is so high that the reverse bias-emitter-base leakage and breakdown voltage are unacceptable for gate-drain characteristics of a JFET. A modified device structure has been developed to alleviate these

TABLE 9. TYPICAL OAT TRANSISTOR PARAMETERS

| Emitter Size | 3(3 μm x 12 μm) | 2(4 μm x 12 μm) | 6.5 μm x 12 μm |
|---|---|---|---|
| Beta | 50 to 200 | 50 to 200 | 50 to 200 |
| $V_{BE}$ at 1 mA | 800 mV | 785 mV | 780 mV |
| $F_T$ (peak) | 4 to 5 GHz | 4 to 5 GHz | 4 to 5 GHz |
| $r_b$ | 72 Ω | 150 Ω | 500 Ω |
| $r_c$ | 80 Ω | 90 Ω | 100 Ω |
| $C_{EB}$ | 0.20 | 0.17 | 0.13 pF at V = 0 |
| $C_{CB}$ | 0.49 | 0.33 | 0.19 pF at V = 0 |
| $C_{CS}$ | 0.23 | 0.17 | 0.12 pF at V = 3 |
| $BV_{EB}$ | 5 V | 5 V | 5 V |
| $BV_{CEO}$ | 8 to 12 V | 8 to 12 V | 8 to 12 V |
| $BV_{CBO}$ | 15 to 25 V | 15 to 25 V | 15 to 25 V |




A. MODIFIED JFET STRUCTURE WITH HIGHER $BV_{GD}$ AND LOWER GATE LEAKAGE

B. STANDARD NPN TRANSISTOR USED AS JFET

Figure 13. P-Channel JFET

problems. This utilizes an extra p diffusion between the normal $p^+$ base (source or drain) and the emitter (gate), as shown in Figure 13a. This extra diffusion is more lightly doped than the normal $p^+$, so as to give a higher breakdown and much lower reverse leakage.

### 4.1.3 JFET Model for Circuit Simulation

The JFET device that has been developed as part of an extended OAT process is not fundamentally different in operation from a discrete p-channel JFET, with the exception that there are additional parasitics as a result of the monolithic construction. The most reasonable approach to a model is to modify a standard JFET model in a circuit simulation program to adequately represent the features of this particular JFET construction. In addition, since the purpose of this project is device development, the model should relate to the physical structure of the device in a fairly direct way so that it can be extrapolated to new device designs or to predict effects of processing variations.

A model that relates directly to the physical structure of the device is shown in Figure 14. All of the model elements except those that are directly connected to the back gate (BG) are part of the SPICE JFET model; the more complete model shown here can be constructed as a subcircuit in the SPICE simulation program.

The controlling equations built into the SPICE program for the p-channel JFET model (SPICE model name PJF) are a set of equations for different operating bias regions. For normal forward operation of the p-channel JFET $V_{DS} < 0$, the equations are

$$I_D = \begin{cases} 0 & (V_{TO} - V_{GS}) < 0 \\ -\beta(V_{GS} - V_{TO})^2 (1 - \lambda V_{DS}) & 0 < (V_{TO} - V_{GS}) < V_{SD} \\ \beta V_{DS}\left[2(V_{GS} - V_{TO}) + \bar{V}_{DS}\right] (1 - \lambda V_{DS}) & 0 < V_{SD} < (V_{TO} - V_{GS}), \end{cases}$$

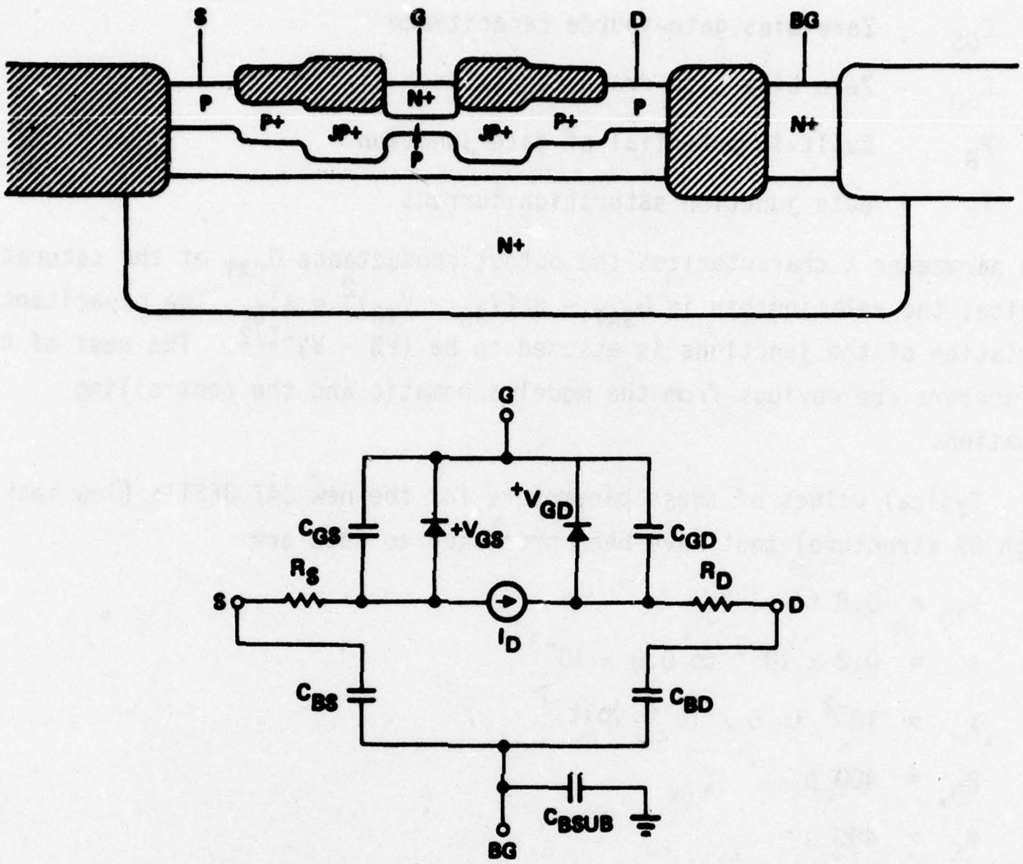



**Figure 14. Physical Structure of JFET Compared to JFET Model**

where the controlling voltages are internal to the model and do not include the ohmic drops in $R_S$ and $R_D$. The input parameters required for the model are

| | |
|---|---|
| $V_{TO}$ | Threshold (or pinchoff) voltage |
| $\beta$ | Transconductance parameter |
| $\lambda$ | Channel length modulation parameter |
| $R_D$ | Drain ohmic resistance |
| $R_S$ | Source ohmic resistance |

$C_{GS}$ Zero bias gate-source capacitance

$C_{GD}$ Zero bias gate-drain capacitance

$P_B$ Built-in potential of gate junction

$I_S$ Gate junction saturation current

The parameter $\lambda$ characterizes the output conductance $G_{SAT}$ of the saturated device; the relationship is $G_{SAT} = \beta\lambda(V_{GS} - V_{TO})^2 \approx \lambda I_D$. The capacitance variation of the junctions is assumed to be $(PB - V)^{-1/2}$. The rest of the parameters are obvious from the model schematic and the controlling equations.

Typical values of these parameters for the new OAT JFET's (low leakage, high BV structure) that have been processed to date are

$V_{TO}$ = -0.8 to -3 V

$\beta = 0.2 \times 10^{-3}$ to $0.8 \times 10^{-3}$

$\lambda = 10^{-2}$ to $5 \times 10^{-2}$ volt$^{-1}$

$R_D$ = 400 Ω

$R_S$ = 400 Ω

$C_{GS}$ = 0.04 pF

$C_{GD}$ = 0.04 pF

$P_B$ = 1.0 V

$I_S = 1 \times 10^{-17}$

Typical values for the additional elements of the subcircuit are

$C_{BD}$ = 0.10 pF

$C_{BS}$ = 0.10 pF

$C_{B_{SUB}}$ = 0.12 pF

Several approximations are involved in the model to limit the number of circuit elements and nodes required for the model. In particular, the parasitic capacitances are lumped approximations to distributed capacitance. The total gate capacitance physically includes gate-source,

gate-drain, and gate-channel capacitance; the gate channel capacitance is the smallest of the three for the short channel devices considered here, so the total gate capacitance is simply split between the elements labeled $C_{GS}$ and $C_{GD}$. Similarly, the back gate capacitance is distributed over the source and drain resistances; it is shown tied to the ends of these resistances to avoid adding extra nodes to the model. The series resistance of the back gate is not included, but it normally would have little effect on circuit performance. The back gate voltage can affect the pinch off voltage ($V_{TO}$) by a small amount. A completely rigorous model would replace the expression ($V_{GS}$ - $V_{TO}$) in the controlling equations by something like ($V_{GS} + \alpha V_{bgs} - V_{TO}$), where $\alpha$ is considerably less than one. For most purposes this is unnecessary, and in any event, $\alpha V_{bgs}$ is generally much smaller than the typical manufacturing variation in $V_{TO}$. The static effects of a fixed $V_{bgs}$ are equivalent to a shift in $V_{TO}$; the dynamic characteristics, if the front and back gates are tied together, is equivalent to a small increase in $g_m$.

Figure 15 shows a comparison of measured JFET transfer characteristics and calculated transfer characteristics of the model. Input parameters for the model were adjusted to fit to the particular device from which the measured data was obtained. The specific model parameters to obtain this matching were beta 9.7 x $10^{-5}$, lambda = 0.032, $V_{TO}$ = 1.25. Other parameters were as listed on the preceding page.

For high accuracy analog circuitry the most important device parameters are usually gate leakage and matching of either pinchoff voltage or $I_{DSS}$. Other significant parameters are transconductance, source resistance, output impedance, and gate-drain breakdown voltage. The principal limitations on frequency reponse are the various parasitic capacitances, particularly the gate capacitance. Some of the performance tradeoffs are made in the device design. The most significant variable is the gate length; increasing the gate length with everything else held constant lowers $g_m$ and $I_{DSS}$, and raises output resistance and gate capacitance so that frequency response is lowered. Changes in gate width merely scale the current level at which the device operates.

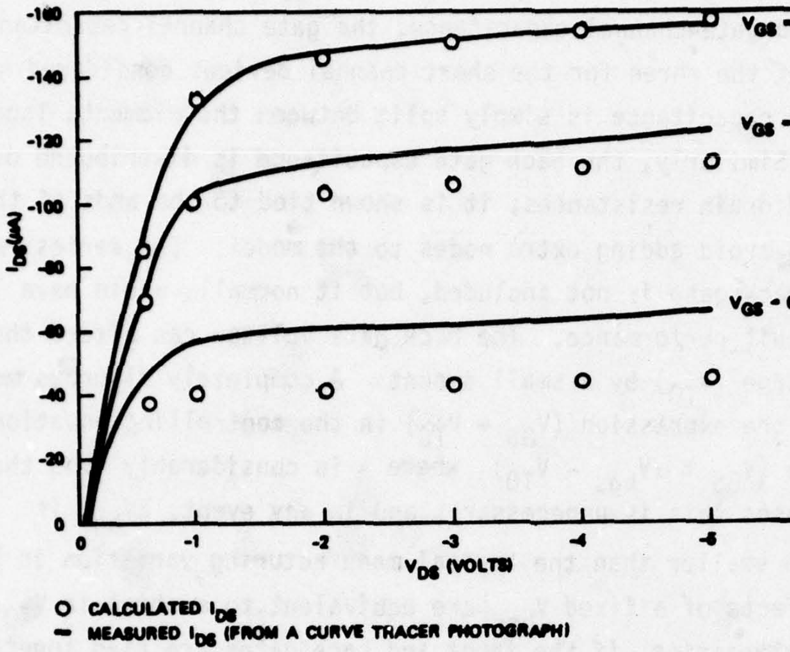



Figure 15. Comparison of JFET Model to Measured Device Characteristics

The quantities that were measured to characterize individual JFETS and JFET pairs include $I_{DSS}$, matching of $I_{DSS}$, pinchoff voltage, $g_m$, gate-drain breakdown voltage, and gate leakage. Gate capacitance was measured on special test structures that are scaled up to provide a large enough capacitance to allow accurate measurements. Special test resistors were utilized to measure source and drain resistances.

The gate capacitance at zero volts was measured on test structures with a total gate width of 4060 μm, with gate lengths of 3 and 5 μm on the mask. The total capacitance of a 3 μm gate was found to be 4 to 5 femto farad (fF) per μm of gate width. Comparison of the data for 3 and 5 μm long gates gives the incremental capacitance as the gate length is increased from 3 μm as 1.3 to 1.4 fF/$\mu m^2$.

The source and drain are made up nominally of a 4 μm length of normal (NPN transistor) $p^+$ diffusion and 4 μm of the special JFET $p^+$ diffusion. The sheet resistance of the normal $p^+$ was measured to be 260 to 280 Ω/sq. The JFET $p^+$ ranged from 600 to 900 Ω/sq over several lots. There is an

additional resistance at the contact to the normal $p^+$ base that is not completely understood, but is approximately equivalent to an additional 3 μm of $p^+$ base. The net source or drain resistance should be about 4900 Ω divided by the total gate width in μm. A minimum geometry device with a gate width of 12 μm should have source and drain resistance of about 400 Ω.

### 4.1.4 Interdigitated JFET Measurements

The basic JFET layout is shown in Figure 8. A number of variations are obviously possible; several of these are compared to the basic device in Figure 16. The basic JFET shown is characterized by the gate length ($L_G$) and width ($W_G = W$). $I_{DSS}$ and $g_m$ vary directly with $W_G$, and approximately inversely with $L_G$. Capacitance to source or drain varies directly with $W_G$, so the maximum slew rate of a source or drain without any external load is independent of $W_G$, but varies approximately inversely with $L_G$. Output impedance decreases with $L_G$. It has been found with the OAT-compatible p-JFETs that gate lengths of less than 4 μm tend to give poor output impedance and poor repeatibility of parameters, but that the 4 μm JFETs are well behaved. Longer gates provide lower output currents (or require a larger device for the same output current) but may be useful when a higher output impedance is desired and the JFET capacitance is not limiting circuit performance.

The layout variations illustrated in Figure 16b, c, d, are principally used to obtain better matching of JFET pairs. The device shown in b can be a common drain (or common source) pair with its gates in close proximity, to obtain good matching. This structure can also be used to make a single JFET with slightly decreased drain (source) to back gate capacitance by tying the two gates together and tying the two sources (drains) together; the next gate width of the device is 2W, but the contact area of the source (drain) is less than is obtained from stretching the basic device to 2W. If the configuration of Figure 16c is used, a more closely matched pair should be obtained since the average $V_{TO}$ of the two sections of G1 should equal that of the two sections of G2 even in the presence of a gradient of $V_{TO}$ across the wafer. This concept can be extended to cancel second order variations in $V_{TO}$ (Figure 16), although this yields a rather large device.

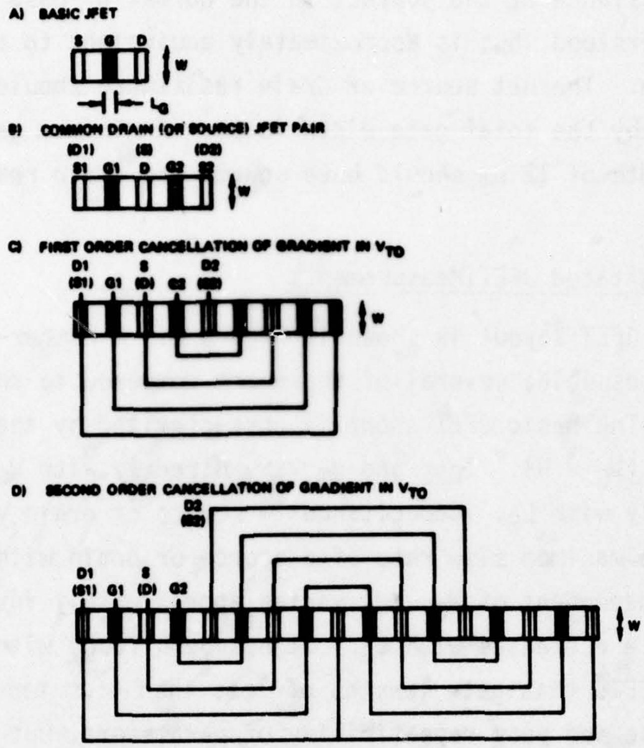



Figure 16. JFET Layout Variations

The majority of the characterization measurements for actual FET devices and device pairs was done on devices with a 4 μm gate length and 48 μm gate width. The variations of pinchoff voltage versus $I_{DSS}$ and $g_m$ for a typical wafer with good JFET processing are shown in Figures 17 and 18. These are representative of the variation to be expected within a wafer. Wafer-to-wafer and lot to lot variation will be considerably larger, but we do not yet have enough experience in processing to set specific limits. Gate to drain breakdown voltage ranged from 7 to above 11 V. Gate leakage for the same devices was measured at room temperature and at 100°C. The total leakage with source and drain tied together and 2.5 V reverse bias applied to the gate ranged from 0.015 to as high as 0.17 nA at room temperature; the average leakage was about 0.05 nA. The leakage at 100°C ranged from 0.3 to 0.8 nA.

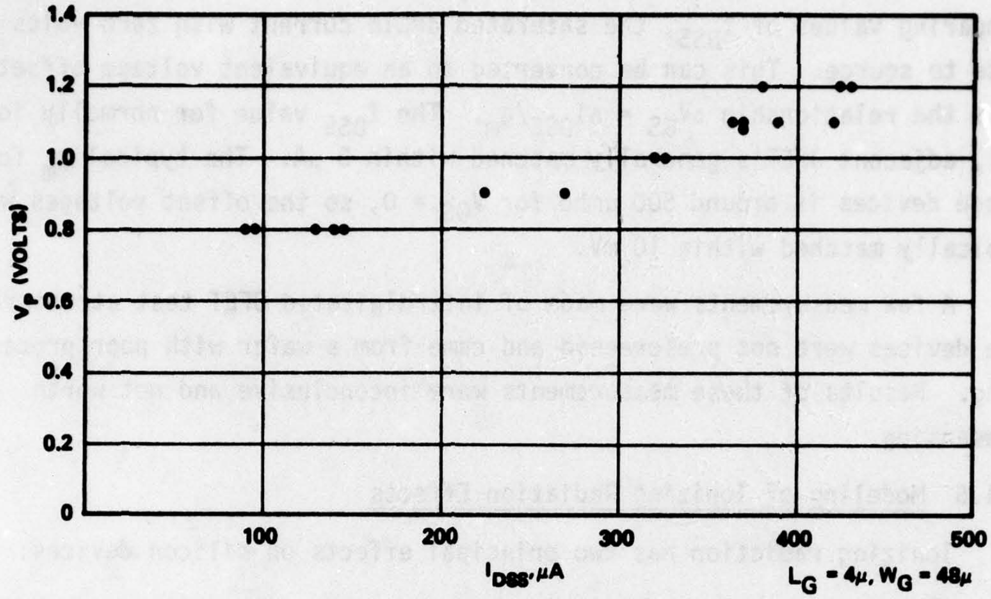



Figure 17. $I_{DSS}$ Versus $V_p$ for Samples from a Single Wafer

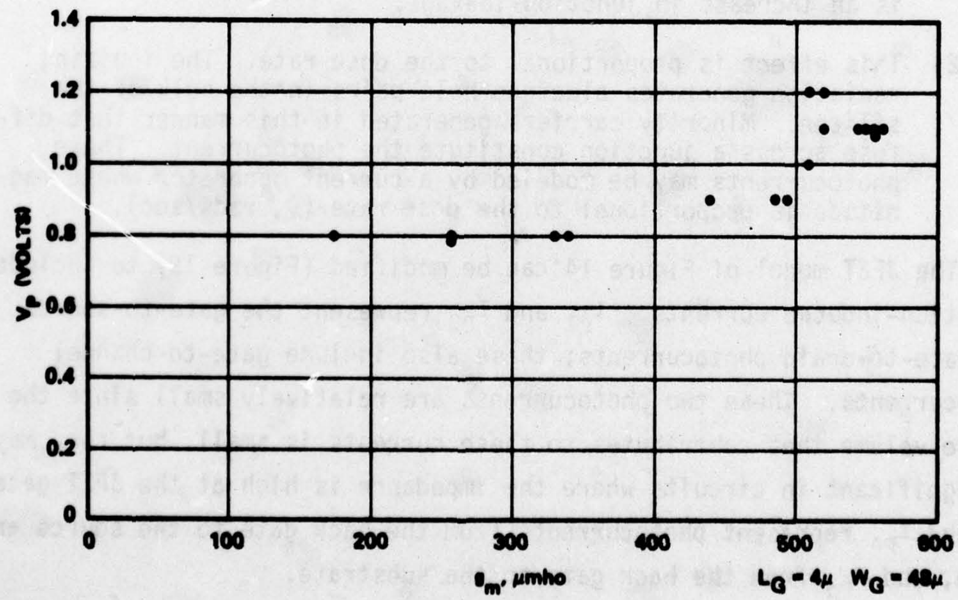



Figure 18. $g_m$ Versus $V_p$ for Samples from a Single Wafer

The degree of matching of pairs of JFETS is most easily measured by comparing values of $I_{DSS}$, the saturated drain current with zero volts from gate to source. This can be converted to an equivalent voltage offset from the relationship $\Delta V_{GS} = \Delta I_{DSS}/g_m$. The $I_{DSS}$ value for normally identical, adjacent JFET's generally matched within 5 μA. The typical $g_m$ for these devices is around 500 μmho for $V_{GS} = 0$, so the offset voltages were typically matched within 10 mV.

A few measurements were made of interdigitated JFET test structures. The devices were not prescreened and came from a wafer with poor processing. Results of these measurements were inconclusive and not worth presenting.

4.1.5 Modeling of Ionizing Radiation Effects

Ionizing radiation has two principal effects on silicon devices:

1) Proportional to the total dose, this effect consists of a buildup of charge at the semiconductor-oxide interface and an increase is the number of surface states; the result is to change the surface potential and generally increase the surface recombination velocity. The FET is a majority carrier device, and the device operation depends principally on potentials within the bulk that are well isolated from the surface, so that the only electrical effect of total ionizing dose observable at the device terminals is an increase in junction leakage.

2) This effect is proportional to the dose rate. The ionizing radiation generates electron-hole pairs in the bulk of the silicon. Minority carriers generated in this manner that diffuse across a junction constitute the photocurrent. These photocurrents may be modeled by a current generator whose magnitude is proportional to the dose rate ($\dot{\gamma}$, rads/sec).

The JFET model of Figure 14 can be modified (Figure 19) to include radiation-induced currents. $I_{P1}$ and $I_{P2}$ represent the gate-to-source and gate-to-drain photocurrents; these also include gate-to-channel photocurrents. These two photocurrents are relatively small since the active volume that contributes to these currents is small, but they may be significant in circuits where the impedance is high at the JFET gate. $I_{P3}$ and $I_{P4}$ represent photocurrents from the back gate to the source and drain, and $I_{P5}$ from the back gate to the substrate.

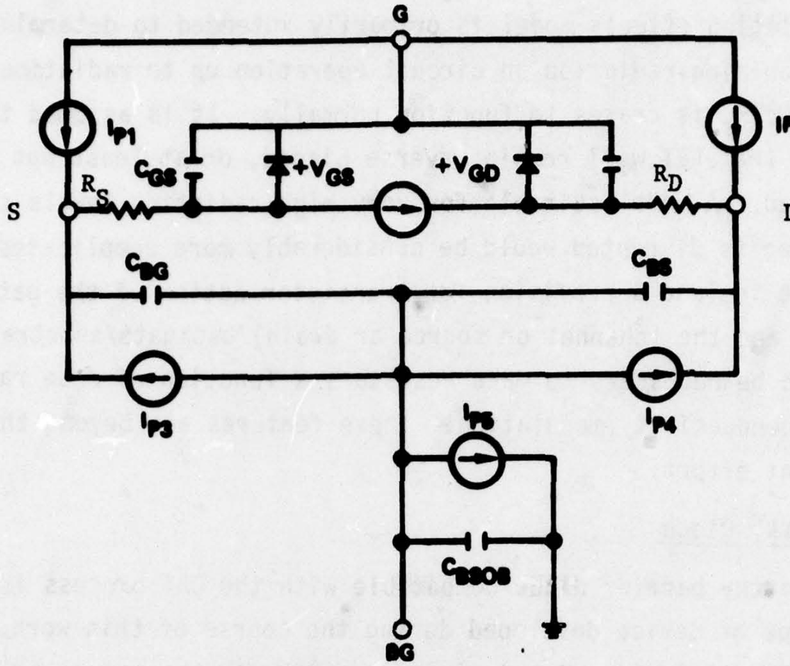



Figure 19. SPICE Subcircuit Form of JFET Model Including Transient Radiation Effects

The constant of proportionality relating the magnitudes of the photocurrent generators is best determined experimentally; no radiation effects measurements have yet been performed on these devices.

One approximation that has been made for convenience is to tie the gate photocurrent generators $I_{P1}$ and $I_{P2}$ directly to the source and drain nodes. The actual photocurrents are in fact injected at the other ends of the source and drain resistance $R_S$ and $R_D$, but currents $I_{P1}$ and $I_{P2}$ are small enough relative to other photocurrents that the circuit will probably have failed before the voltage droop across $R_S$ and $R_D$ from the gate photocurrents becomes significant. If it were deemed desirable to do so, a slightly more accurate model may be obtained at the expense of two additional nodes in the JFET subcircuit by setting $R_S$ and $R_D$ in the JFET model to zero and adding source and drain resistors to the subcircuit external to the model. Photocurrent generators $I_{P1}$ and $I_{P2}$ can then be connnected inside these source and drain resistors.

The radiation effects model is primarily intended to determine the effects of ionizing radiation on circuit operation up to radiation levels at which the circuit ceases to function normally. It is assumed that all junctions in the JFET will remain reverse biased, or at least not heavily forward biased. A model suitable for very high radiation levels such that normal biasing is disrupted would be considerably more complicated, as it would need to include a provision for transistor action of the gate/channel/backgate npn and the (channel or source or drain)/backgate/substrate pnp. It would also be necessary to make resistors a function of dose rate to account for conductivity modulation. These features are beyond the scope of the present effort.

4.1.6 Schottky Diode

The Schottky barrier diode compatible with the OAT process is the other new type of device developed during the course of this work. The contact to the metal side of the diode is made with the normal interconnect metallization. The contact to the semiconductor side is made through buried layer diffusion and a normal collector contact (see Figure 7).

The circuit application for the Schottky barrier diode in a sample and hold circuit is usually as a fast switch. The most important parameters are usually diode series resistance, parasitic capacitance, and leakage current. Since the Schottky barrier diode is a majority carrier device, the inherent switching time is usually negligible compared to other circuit time constants. For differential circuitry, it is also important to know the matching of the diodes.

The series resistance of the diode consists of a vertical resistance through the epi, the resistance of the buried layer from under the diode to the collector contact, and a small contribution from the contact itself. Also, there is a contribution from the current voltage characteristics of the diode that is equivalent to a resistance of $(nkT)/(qI_D)$ where $I_D$ is the diode current, $kT/q$ is about 26 mV at room temperature, and n describes the deviation from ideal diode characteristics. An ideal p-n junction diode has $n \simeq 1.00$; the best silicon Schottky diodes have $1.02 \leq n \leq 1.05$, but n can be as large as 1.5 or 2 for very poor diodes.

The parasitic capacitance includes the depletion capacitance of the diode and the capacitance to the substrate of the buried layer and collector contact areas that form the cathode side of the diode.

Two sizes of diodes, designated 1x and 2x, were fabricated and characterized. The 1x diode has an anode dimension of 20 μm x 24 μm on the mask, which gives an effective area for the processed diode of about 17 μm x 21 μm, or 357 $\mu m^2$. The 2x diode has mask dimensions of 40 μm x 24 μm, so the effective size is 37 μm x 21 μm or 777 $\mu m^2$. A typical forward I-V characteristic for a Schottky diode is shown in Figure 20. The series resistance and ideality factor n can be obtained by substracting an IR drop from the diode voltage and choosing the value for R that gives the best fit to $(V_F - IR) = nkT/q[\ln(I_f/I_C)]$. For this case n = 1.08 and the best estimate of the ohmic series resistance is 24 Ω. A special test structure with the same dimensions as the 1x Schottky diode but with emitter diffusion in place of the Schottky barrier was used to independently estimate the series resistance. This gave 22 Ω on the same wafer from which the diode voltage data was taken, and ranged from 22 to 66 Ω over a number of wafers.

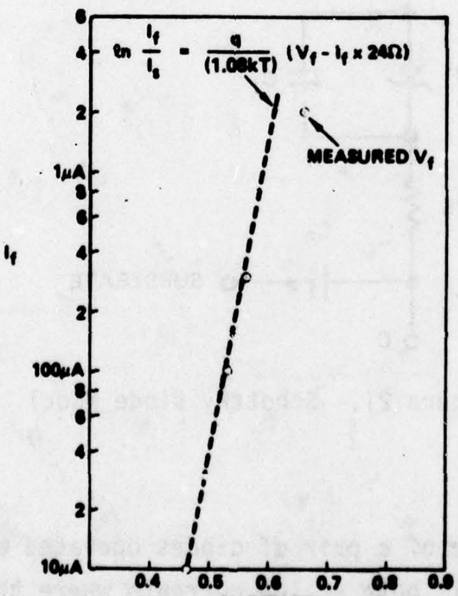



Figure 20. Schottky Diode I-V Characteristics

The reverse leakage of a number of 1x diodes was measured at 2 V reverse bias and found to range from 0.05 to 0.3 nA at room temperature, with typical value of 0.1 nA. At 100°C, the range was 0.45 to 1.7 nA, with a typical value of 1.1 nA.

The junction capacitance of an individual diode is small enough as to be difficult to measure accurately, so a large area diode 335 μm x 336 μm was fabricated and measured to obtain the junction capacitance. At zero bias the capacitance measured was 0.0003 to 0.0004 pf/μm$^2$. This gives a junction capacitance of 0.13 pf for the 1x diode and 0.28 pf for the 2x diode. The cathode to substrate capacitance is more difficult to obtain since it is dependent on both area and perimeter of the diode, and because it is difficult to separate the parasitic capacitance of the measurement setup from the desired substrate capacitance. The capacitance is estimated to be about 0.12 pf for the 1x diode and 0.17 pf for the 2x diode.

The circuit model for the diode is shown in Figure 21. Typical element values are listed in Table 10.

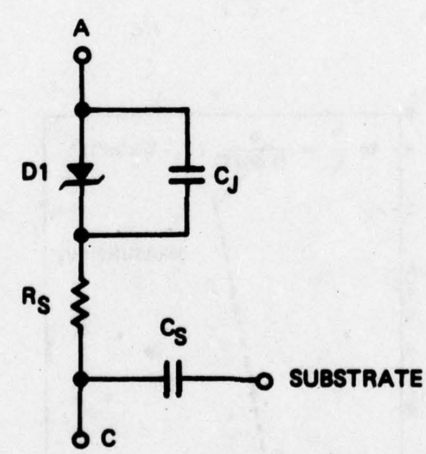



Figure 21. Schottky Diode Model

### 4.1.7 Diode Matching

The forward voltage of a pair of diodes operated at the same current tends to match quite well both at low currents where the operation is dominated by the actual diode characteristics, and at high currents where the series resistance begins to contribute a significant part of the voltage droop.

TABLE 10. ELEMENT VALUES FOR 1x SCHOTTKY DIODE MODEL

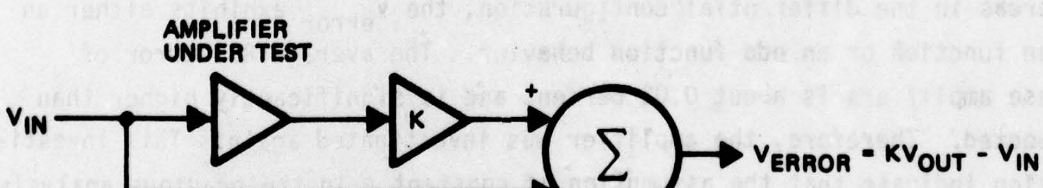
| Element | Typical Value | |
|---|---|---|
| $C_J$ | 0.12 pf | [included in SPICE diode model] |
| $R_S$ | 40 Ω | |
| D1 | $I_S = 5 \times 10^{-13}$ amp/cm$^2$<br>N = 1.08 | |
| $C_S$ | 0.13 pf | [to be added external to SPICE model] |

## 4.2 BASIC AMPLIFIER EVALUATION

Twelve amplifier circuits were tested for their dc linearity, and one chip was further tested for its harmonic distortion at 7.6 MHz. The dc linearity of this amplifier is about 0.02 percent and its second harmonic is at least 60 dB down from the fundamental frequency at 7.6 MHz. The nonlinearity is five times higher than expected. The cause of this unexpected nonlinearity was found to be the beta or alpha dependence on the transistor's instantaneous collector current. The 0.02 percent linearity is adequate for most 10 bit A/D converter applications.

### 4.2.1 DC Linearity Test Results

To test dc linearity efficiently, a special test box was built. The principle of operation of this box is very simple and is illustrated below.




If K is adjusted such that it is the reciprocal of the least square gain of the amplifier under test, $V_{error}$ will be the nonlinearity of the amplifier at a given input.

This test box is designed such that a 10$\mu$V error can easily be resolved. Twelve chips were tested and the maximum errors, $|V_{error}|_{max}$, for these amplifiers in different output configurations are given in Table 11. Input: $V_{IN}$ = 0.8 sin $2\pi$ ft volts, f = 0.05 Hz (single-ended).

TABLE 11. $|V_{ERROR}|_{MAX}$

| Output Configurations / $\lvert V_{error}\rvert_{max}$ (mV) / Chip No. | Single | Differential |
|---|---|---|
| 1 | 0.75 | 0.1 |
| 2 | 0.65 | 0.35 |
| 3 | 0.5 | 0.4 |
| 4 | 0.9 | 0.4 |
| 5 | 0.65 | 0.45 |
| 6 | 0.75 | 0.5 |
| 7 | 1.2 | 0.5 |
| 8 | 0.4 | 0.65 |
| 9 | 0.7 | 0.6 |
| 10 | 0.1 | 0.9 |
| 11 | 1.0 | 1.5 |
| 12 | 1.5 | 1.8 |

Of the 12 chips investigated, seven have better linearity when operating in the differential output configuration. When the amplifier output is single-ended, the $V_{error}$ exhibits an even function behavior. Whereas in the differential configuration, the $V_{error}$ exhibits either an even function or an odd function behavior. The average RSS error of these amplifiers is about 0.02 percent and is significantly higher than expected. Therefore, the amplifier was investigated again. This investigation indicate that the assumption of constant $\beta$ in the previous analysis is invalid. After putting realistic $\beta$ variations into the analysis, a close correlation between measurement and theory is obtained.

### 4.2.2 Harmonic Distortion Test Results

Chip 7 was used for the harmonic distortion test by a spectrum analyzer. A 7.6 MHz sinewave with 1.6 Vpp is used as the input. To match the amplifier output impedence to a 50 Ω system, a wideband transformer (Vari-L HF128) is used for impedance transformation. The data is listed below.

| Configuration | Normalized Second Harmonic |
|---|---|
| Single-ended input/Single-ended output | -62 dB |
| Single-ended input/Differential output | -69 dB |
| Differential input/Single-ended output | -65 dB |
| Differential input/Differential output | -70 dB |

From the spectrum analyzer displays of the amplifier output spectra, there was only a second harmonic component. The third harmonic was down at least 80 dB. From the dc linearity measurement of chip 7, the $V_{error}$ has a definite square law behavior, so the presence of a second harmonic is not surprising.

### 4.2.3 Frequency Response Test Results

Chip 7 was also used for the frequency response tests. These tests indicated that the frequency response is dominated by the output load capacitance and resistance, therefore a more realistic measurement of frequency response of this amplifier is to measure the transadmittance (gm) of the amplifier.

Test results indicated that the amplifier gain was constant up to 1 GHz.

### 4.2.4 Conclusion

For the linearity test and harmonic distortion test, the single-end output configuration generally exhibits second harmonic or parabolic error voltage ($V_{error} = V_{IN} - V_{OUT}$). The differential output configuration exhibits parabolic or cubic error voltage. With no design changes this amplifier exhibits an accuracy of an ideal 8 bit device. The cause of the nonlinearity was analyzed in detail; the results of the analysis

indicated that in the single-ended output configuration, nonlinearity is primary due to npn transistor alpha dependence on its collector current; while the main cause of nonlinearity in a differential output configuration is still uncertain. One possible cause might be device mismatch. Without circuit changes the linearity of this amplifier can be improved by increasing the device size and reducing the input voltage range such that the alphas will have less variation, thus better linearity.

### 4.3 SHD-1 SAMPLE AND HOLD TESTS

The test data for the bipolar version of the sample and hold is summarized in Table 12. This data indicates that the main problem in achieving good performance is the third harmonic level. This level is dependent upon the acquisition time and is primarily caused by a nonlinear hold jump. The hold jump is a nonlinear function of the input voltage level.

The sample and hold exhibits excellent hold characteristics with a maximum droop over temperature of 0.25 mV/120 nsec, this performance is adequate for 10 bit A/D converters. The SNR tests were performed by measuring the ratio of signal power to noise power of the sample and hold output with the sample and hold sampling at 25 Msps. A plot of SNR versus track time and input amplitude is shown in Figure 22. The sample and hold has higher SNR when it has longer track time. This indicates that the acquisition time is influencing the sample and hold output. From earlier testing data, the sample and hold acquisition time was determined to be about 11 nsec. The long acquisition time is the result of the high cermet sheet resistance on the first lot of wafers (350 Ω/sq versus design of 200 Ω/sq). Since acquisition time is related to RC time constant, a 50 percent increase in resistance implies a 50 percent increase in acquisition time, for which the 11 nsec acquisition time is well within the predicted performance.

The sample and hold test setups and test data are presented in the appendix.

TABLE 12. SHD-1 SAMPLE AND HOLD RESULTS

| Test | Performance | Test Conditions |
|---|---|---|
| SNR | 52 dB | 25 Msps<br>10 MHz NBW<br><br>10 nsec Track<br>1.6 V p-p single-ended Input/Output<br>$f_{in}$ = 7.6 MHz |
| Harmonic Distortion | 53 dB | Third Harmonic of 7.6 MHz<br>11 nsec Track Time |
| Hold Jump Linearity | 7 mV pp | 5 Msps<br>10 nsec Track Time<br>1.6 V p-p Output<br><br>Relates to 53 dB Signal to Noise |
| Third Harmonic Versus Acquisition Time | | 25 Msps<br>$f_{in}$ = 7.6 MHz<br>1.6 V p-p Input |
| 15 nsec | 61 dB | |
| 10 nsec | 55 dB | |
| 5 nsec | 44 dB | |
| Droop | 0.25 mV/120 nsec | -25 to +100°C tested over entire 1.6 V signal range |

## 4.4 A/D CONVERTER TESTS

The complete sample and hold circuit (bipolar option) was tested with the aid of an ADC-4 8 bit successive approximation quantizer. The SHD-1 and ADC-4 were connected to form an A/D converter. Tests were performed by measuring the conversion noise of the sample and hold circuit and the quantizer, and comparing that to the conversion noise of the quantizer alone. The test results are shown in the graph in Figure 23 and data is

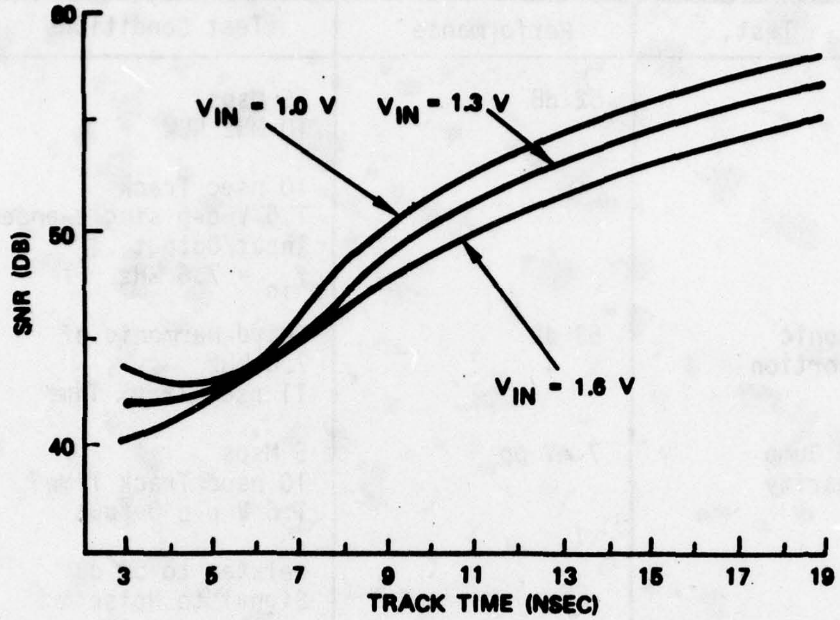



**Figure 22. Sample and Hold SNR Performance**

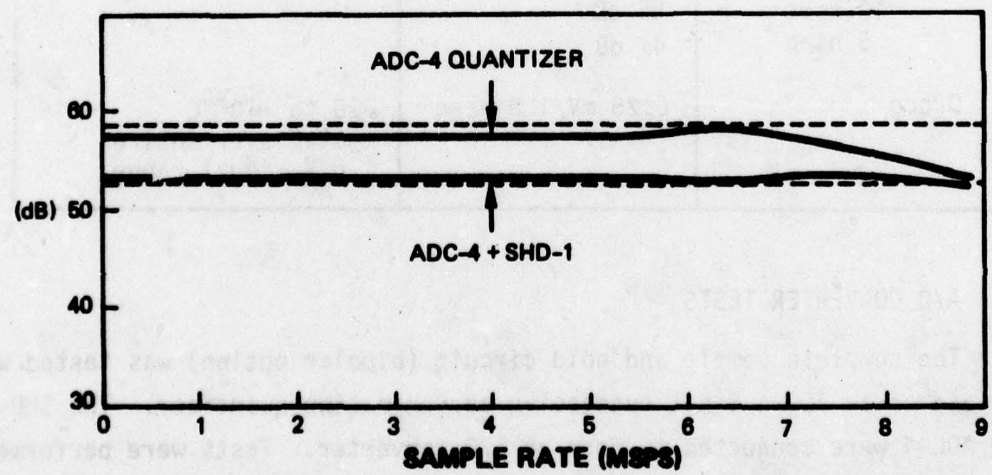



**Figure 23. Conversion Noise of SHD-1 (Bipolar Version)**

given below in Table 13. The test data indicates that the sample and hold causes approximately 5 dB degradation indicating that it is adequate for 7 bit analog-to-digital conversion applications.

TABLE 13. A/D TEST RESULTS

| Sample Frequency (MHz) | Bit Clock Frequency (MHz) | Conversion Noise | |
|---|---|---|---|
| | | ADC-4 (dB) | ADC-4 + SHD-1 (dB) |
| 1.1 | 10 | 57.7 | 53.3 |
| 4.4 | 40 | 57.7 | 52.9 |
| 5.5 | 50 | 57.7 | 53.3 |
| 6.6 | 60 | 58.3 | 53.1 |
| 7.8 | 70 | 55.8 | 53.4 |
| 8.9 | 80 | 53.5 | 52.5 |

## 5. CONCLUSIONS AND RECOMMENDATIONS

The devices necessary to develop a fully monolithic sample and hold (S/H) circuit have been successfully incorporated in the OAT process. Tests of these devices indicate that they meet the program goals and that they can be used in a monolithic S/H circuit. Tests of the S/H building blocks and the complete circuit have proven that the process, devices, and circuits will produce a useful S/H circuit. The S/H circuit evaluated is far from optimum, being a test and evaluation device; however, it is useful in its present form for 7 to 9 bit applications.

It is recommended that the development of the monolithic S/H be continued to improve the performance and optimize the circuits and monolithic process. Specific processing improvements need to be realized in the formation of the channel stop. In particular it is recommended that the channel stop be formed by ion implantation instead of diffusion. This development should be followed by the development of a single chip monolithic A/D converter which includes the S/H and quantizer circuitry.

## REFERENCES


1. L.W. Hobrock, "Low Power Radiation Hardened Analog-to-Digital Converter," AFAL-TR-75-204, Vol. II, TRW Systems Group.

2. Braun and Lood, "Precision Thin Film Cermet Resistors for Integrated Circuits," Proc. IEEE, Vol. 54, 1966, pp. 1521-1527.

## APPENDIX
## SAMPLE AND HOLD TEST SETUPS AND TEST DATA

**TEST CONDITIONS**

- **All bipolar transistors**
- **On-chip 1 pf hold-capacitor**
- **No bootstrapping in the post-amplifier input emitter followers**
- **Preamplifier is not switching.**

TITLE: Sample and Hold Droop Rate

PURPOSE: To investigate the bipolar sample and hold droop rate versus temperature and input voltage.

## TEST SETUP

- Droop is initially compensated at +25 C and $V_{IN}$ = 0 volt. Then the test was performed without any further adjustment.
- Chip 3/21/4/5 was measured. (Regular OAT with Schottky diodes, the sampling diodes are P-N junction type.)
- Hold capacitance of the SHD-1 is comprised of two elements:

  1) On-chip hold capacitor (≈1 pf)

  2) Package lead capacitance (≈3 pf)

  Test Result: Track time = 50 nsec

  Hold time = 150 nsec

## TEST RESULTS

| Droop (mV) / Temp / $V_{IN}$ | 100°C | 75°C | 50°C | 25°C | 0°C | -25°C |
|---|---|---|---|---|---|---|
| 0.8 | * | 0 | 0 | 0 | 0 | 0 |
| 0.4 | +0.5 | -0.5 | -0.2 | -0.2 | -0.2 | -0.2 |
| 0 | -0.2 | 0 | -0.5 | 0 | -0.2 | 0 |
| -0.4 | 0 | 0 | -0.2 | -0.5 | -0.5 | -0.2 |
| -0.8 | 0 | 0 | +0.2 | -0.5 | 0 | 0 |

*no data taken

**TITLE**: Tracking Sample and Hold Harmonic Distortion and SNR

**PURPOSE**: To investigate the sample and hold harmonic distortion and SNR when it is in track-only mode.

## TEST SETUP

A block diagram of the test set up is shown in Figure A-1. The SHD-1 is set up such that it always has differential input and single-end output. Also the basic amplifier is used as a buffer for the SHD-1 because the sample-and-hold cannot drive a low impedence load. Both the SHD-1 input and the basic amp output used a wide-band transformer for impedence translation as well as dc isolation. The basic amplifier has linearity better than 70 dB such that its usage as a buffer will not introduce any significant error. So the noise and distortion measured after the basic amplifier will be contributed by the sample-and-hold rather than the basic amplifier.

## TEST RESULTS

Even using 2 AV4, the noise of the sample and hold is still too low for the rms meter. Therefore, there is no SNR and distortion data for tracking sample and hold. However, the SNR and harmonic distortion for tracking sample and hold should be greater than 65 dB (the noise floor of the testing system).

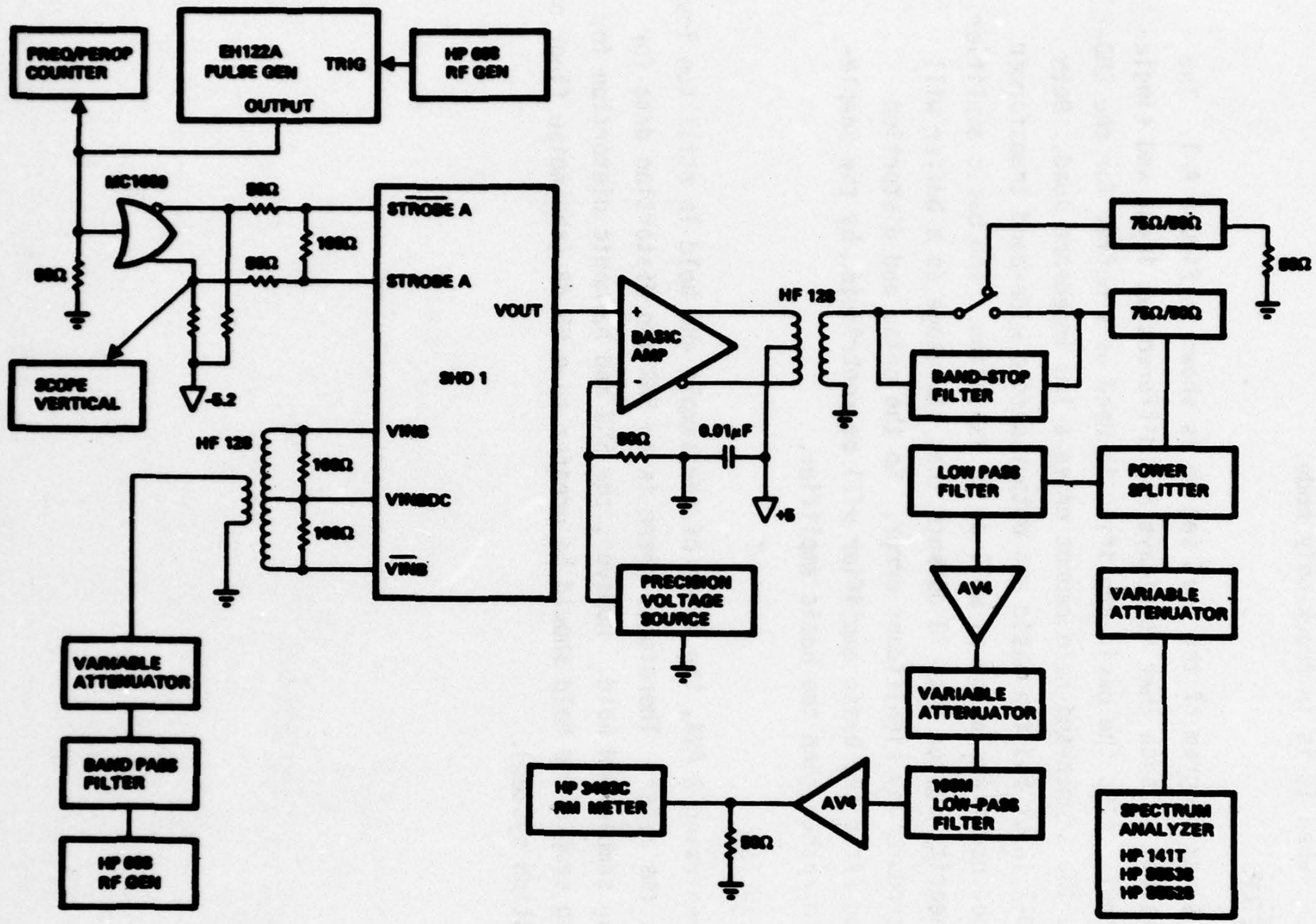



Figure A-1. SNR and Harmonic Testing Setup

TITLE: Sample and Hold Hold Jump Linearity

PURPOSE: To investigate the sample and hold hold jump linearity

TEST SETUP

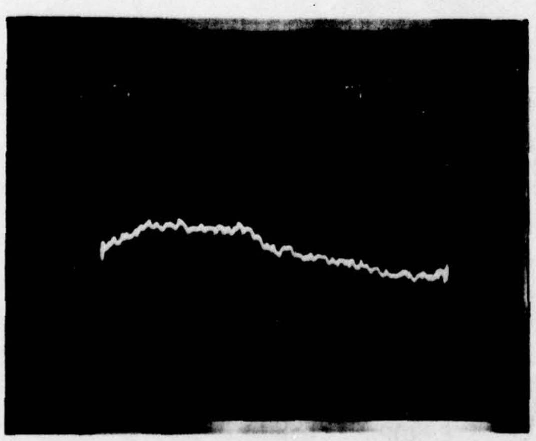
The SHD-1 is housed in a test fixture with proper voltage supplies. The SHD-1 is configured in a single-ended input/output configuration. The hold jump nonlinearity is obtained by subtraction performed by the dc linearity test box used for testing the linear amplifier. The nonlinearity is displayed on the scope.

TEST RESULTS

The sample and hold linearity in the track mode is shown in Figure A-2. The linearity while sampling is shown in Figure A-3 for three different track periods at a constant 5 MHz sample rate.

The sample and hold hold jump nonlinearity exhibits behavior of an odd function $\left[\text{i.e., } V_{OUT} = a_1 V_{IN} + a_3 V^3_{IN} + a_5 V^5_{IN} + a_7 V^7_{IN} + \ldots\right]$. The sample and hold nonlinearity introduced by the hold jump is quite considerable. The sample and hold SNR based only on the hold jump nonlinearity will yield a SNR equal to 53, 57, and 62 dB for track time equal to 10, 20, and 50 nsec respectively.

TEST RESULT



S/H configuration: single ended input/output

$V_{IN} = 0.8 \sin 2\pi ft$, f = 0.05 Hz

Display = 200 $V_{ERROR}$ = 200 [ $KV_{IN} - V_{OUT}$]
$K \simeq 1$

Horizontal scale: Top right number
Vertical scale: Top left number

$V_{ERROR_{max}}$ = 0.6 mV p-p

$RSS_{ERROR}$ = 0.038% (69 dB)

Figure A-2. SHD-1 Linearity is in Track Mode

**TEST RESULT**

S/H configuration: single-ended input/output

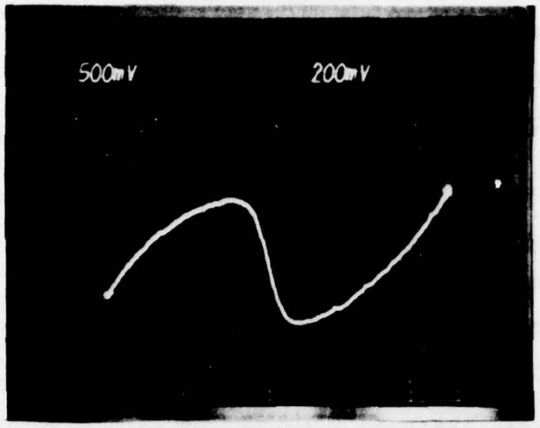
$V_{IN} = 0.8 \sin 2\pi ft$, $f = 0.05$ Hz

$f_s = 5$ MHz $\quad K \simeq 1$

Display = 200 $V_{ERROR}$ = 200 $[KV_{IN} - V_{OUT}]$

Horizontal scale: Top right number

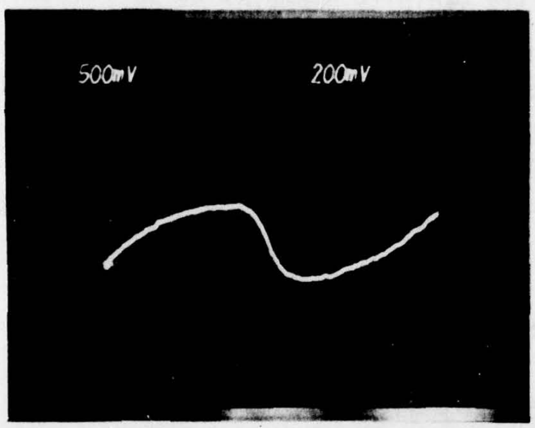
Vertical scale = Top left number




Track Time = 10 nsec

$V_{ERROR_{max}}$ = 7 mV p-p

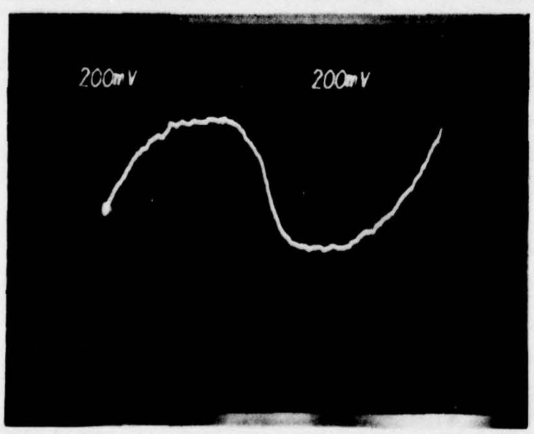
$RSS_{ERROR}$ = .22% (53 dB)




Track Time = 20 nsec

$V_{ERROR_{max}}$ = 4.5 mV p-p

$RSS_{ERROR}$ = 0.14% (57 dB)




Track Time = 50 nsec

$V_{ERROR_{max}}$ = 2.7 mV p-p

$RSS_{ERROR}$ = 0.084% (62 dB)

Figure A-3. SHD-1 Hold Jump Linearity

**TITLE:** Sampling Sample and Hold Harmonic Distortion and SNR

**PURPOSE:** To investigate the sample and hold harmonic distortion and SNR when it is in sampling mode.

**TEST SETUP**

The setup is same as that for the sample and hold frequency domain test in the track mode.

**TEST RESULTS**

**Conditions:** $f_{in}$ = 7.6 MHz  $f_s$ = 25 MHz  $\boxed{V_{in} = 1.6 \text{ V p-p}}$

BW = 10 MHz

| Track Time (nsec) | Normalized Third Harmonic Amplitude (dB) | RMS Signal (mV) | RMS Noise (mV) | SNR (dB) |
|---|---|---|---|---|
| 3 | 41 | 325 | 3 | 40.7 |
| 5 | 44 | 434 | 3.17 | 42.7 |
| 7 | 48 | 467 | 2.29 | 46 |
| 9 | 53 | 486 | 1.47 | 50.4 |
| 11 | 57 | 495 | 1.05 | 53.4 |
| 13 | 61 | 501 | 0.898 | 54.9 |
| 15 | 62 | 509 | 0.788 | 56.3 |
| 17 | 63 | 514 | 0.703 | 57.3 |
| 19 | 64 | 520 | 0.626 | 58.4 |

**Condition:** $f_{in}$ = 7.6 MHz $f_s$ = 25 MHz $\boxed{V_{in} = 1.3 \text{ V p-p}}$

BW = 10 MHz

| Track Time (nsec) | Normalized Third Harmonic Amplitude (dB) | RMS Signal (mV) | RMS Noise (mV) | SNR (dB) |
|---|---|---|---|---|
| 3 | 43 | 265 | 2.03 | 42.3 |
| 5 | 44 | 355 | 2.52 | 42.9 |
| 7 | 47 | 382 | 2.00 | 45.6 |
| 9 | 52 | 396 | 1.38 | 49.2 |
| 11 | 55 | 404 | 1.06 | 51.6 |
| 13 | 57 | 408 | 0.898 | 53.2 |
| 15 | 60 | 414 | 0.740 | 55 |
| 17 | 61 | 420 | 0.696 | 55.6 |
| 19 | 62 | 423 | 0.59 | 57.1 |

**Condition:** $f_{in}$ = 7.6 MHz $f_s$ = 25 MHz $\boxed{V_{in} = 1.0 \text{ V p-p}}$

BW = 10 MHz

| Track Time (nsec) | Normalized Third Harmonic Amplitude (dB) | RMS Signal (mV) | RMS Noise (mV) | SNR (dB) |
|---|---|---|---|---|
| 3 | 46 | 205 | 1.30 | 44 |
| 5 | 44 | 276 | 1.93 | 43.1 |
| 7 | 47 | 300 | 1.61 | 45.4 |
| 9 | 51 | 309 | 1.22 | 48.1 |
| 11 | 54 | 314 | 0.971 | 50.2 |
| 13 | 57 | 319 | 0.825 | 51.7 |
| 15 | 59 | 323 | 0.696 | 53.3 |
| 17 | 60 | 327 | 0.632 | 54.3 |
| 19 | 62 | 329 | 0.547 | 55.6 |

From the trends of the normalized third harmonic amplitude, the acquisition time of the sample and hold is about 13 nsec, an increase of 80 percent over the design value. This is due to the 80 percent increase of the cermet sheet resistance. With increasing track time, the SHD-1 has better SNR. This can be attributed to the long acquisition of the sample and hold. There is a direct correlation between the measured SNR with the predicted SNR based on hold jump nonlinearity. This leads to the conclusion that the dominant cause of the sample and hold nonlinearity is the nonlinear hold jump, for a fully acquired sample and hold.

**TITLE:** Sample and Hold Harmonic Distortion Versus Duty Cycle

**PURPOSE:** To investigate the sample and hold harmonic distortion when it has different duty cycle by varying the sampling frequency while maintaining fixed track time.

## TEST SETUP

The setup is the same as that for the tracking sample and hold frequency domain test except no bandstop filter is used. Care is taken into the selection of different duty-cycles. Selection is made such that each adjacent sampling has the same voltage difference so other time-domain effects like slewing will not interfere with the investigation of sample and hold harmonic distortion versus different duty cycle. Futhermore the numerical data for amplitudes of the harmonics should not be taken as an absolute number because the spectrum analyzer does not yield correct harmonics amplitude information when a big fundamental is present. However, the trend of harmonics versus different duty cycles can be extracted without any degradation.

Conditions: The input frequency $f_{in} = 7.6$ MHz

$V_{in} = 1.6$ V p-p

## TEST RESULTS

Generally, most of the harmonic amplitudes decrease with an increase of track time because of the acquisition problem of the sample and hold. The amplitudes of odd harmonics remain constant independent of the hold time. This could be explained by the fact that all odd harmonics are generated by nonlinear hold jumps, and hold jumps do not change with the length of the hold time. However, the even harmonic amplitudes increase with hold time. This might be due to the fact that the hold droop is introducing additional nonlinearity, when the hold time is significant for the sample and hold.

HARMONIC OF INTEREST: SECOND

| AMPLITUDE (dB) / TRACK TIME / SAMPLING PERIOD (nsec) | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | 48 | 57 | 61 | 61 | 66 | 68 | 68 | * |
| 227 | 47 | 56 | 59 | 61 | 66 | 64 | 66 | 67 |
| 409 | 55 | 56 | 58 | 60 | 63 | 64 | 64 | 64 |
| 541 | 42 | 56 | 58 | 57 | 59 | 59 | 60 | 61 |
| 672 | 36 | 50 | 56 | 56 | 54 | 56 | 56 | 58 |
| 804 | 31 | 45 | 52 | 54 | 54 | 54 | 54 | 54 |

*No data because amplitude is too small to measure

HARMONIC OF INTEREST: THIRD

| AMPLITUDE (dB) / SAMPLING PERIOD (nsec) \ TRACK TIME | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | 36 | 41 | 43 | 46 | 47 | 47 | 48 | 48 |
| 227 | 36 | 40 | 42 | 46 | 48 | 47 | 48 | 49 |
| 409 | 35 | 40 | 42 | 46 | 47 | 48 | 48 | 49 |
| 541 | 35 | 39 | 42 | 46 | 48 | 47 | 48 | 50 |
| 672 | 36 | 40 | 42 | 46 | 43 | 47 | 48 | 50 |
| 804 | 38 | 40 | 43 | 46 | 48 | 47 | 48 | 50 |

HARMONIC OF INTEREST: FOURTH

| AMPLITUDE (dB) / TRACK TIME / SAMPLING PERIOD (nsec) | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | 62 | 65 | * | * | * | * | 64 | * |
| 227 | 66 | 66 | * | * | * | * | 65 | * |
| 409 | 61 | * | * | * | * | * | * | * |
| 541 | 50 | 63 | 67 | 70 | * | 68 | 67 | * |
| 672 | 45 | 56 | 61 | 69 | 68 | 64 | 64 | 63 |
| 804 | 42 | 50 | 55 | 62 | 65 | 60 | 60 | 60 |

*No data because amplitude is too small to measure

HARMONIC OF INTEREST: FIFTH

| AMPLITUDE (dB) / TRACK TIME / SAMPLING PERIOD (nsec) | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | 49 | 50 | 51 | 54 | 56 | 54 | 54 | 54 |
| 227 | 48 | 49 | 51 | 54 | 56 | 54 | 54 | 53 |
| 409 | 48 | 49 | 50 | 54 | 56 | 53 | 54 | 53 |
| 541 | 48 | 48 | 50 | 54 | 56 | 54 | 53 | 53 |
| 672 | 52 | 49 | 50 | 54 | 56 | 54 | 54 | 53 |
| 804 | 57 | 50 | 51 | 54 | 55 | 54 | 54 | 54 |

HARMONIC OF INTEREST: SIXTH

| AMPLITUDE (dB) / TRACK TIME / SAMPLING PERIOD (nsec) | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | ** | * | * | * | * | 69 | * | * |
| 227 | ** | * | * | * | * | * | * | * |
| 409 | 64 | ** | ** | * | 70 | * | * | * |
| 541 | 56 | 63 | 66 | 70 | * | * | * | * |
| 672 | 54 | 57 | 59 | 64 | 66 | 66 | 65 | * |
| 804 | 55 | 54 | 56 | 66 | 62 | 62 | 62 | * |

*No data taken

**No data because amplitude is too small to measure

HARMONIC OF INTEREST: SEVENTH

| AMPLITUDE (dB) / TRACK TIME / SAMPLING PERIOD (nsec) | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | 58 | 56 | 56 | 57 | 58 | 57 | * | 58 |
| 227 | 56 | 55 | 54 | 56 | 58 | 56 | * | 57 |
| 409 | 56 | 54 | 54 | 56 | 56 | 55 | * | 57 |
| 541 | 61 | 54 | 54 | 56 | 58 | 56 | * | 56 |
| 672 | 66 | 56 | 55 | 56 | 56 | 56 | * | 56 |
| 804 | 57 | 59 | 56 | 57 | 56 | 56 | * | 56 |

*No data taken

HARMONIC OF INTEREST: EIGHTH

| AMPLITUDE (dB) / SAMPLING PERIOD (nsec) \ TRACK TIME | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | ** | * | * | * | * | 69 | * | * |
| 227 | ** | * | * | * | * | * | * | * |
| 409 | 64 | * | * | * | 70 | * | * | * |
| 541 | 56 | 63 | 66 | 70 | * | * | * | * |
| 672 | 54 | 57 | 59 | 64 | 66 | 66 | 65 | * |
| 804 | 55 | 54 | 56 | 66 | 62 | 62 | 62 | * |

*No data taken

**No data because amplitude is too small to measure

HARMONIC OF INTEREST: NINETH

| AMPLITUDE (dB) / TRACK TIME / SAMPLING PERIOD (nsec) | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | 60 | 58 | 58 | 60 | * | 60 | 61 | 52 |
| 227 | 58 | 57 | 57 | 59 | * | 59 | 62 | 52 |
| 409 | 57 | 56 | 57 | 58 | * | 61 | 60 | 51 |
| 541 | 58 | 56 | 56 | 58 | * | 58 | 62 | 64 |
| 672 | 61 | 59 | 57 | 60 | * | 59 | 61 | 64 |
| 804 | 58 | 58 | 59 | 60 | * | 58 | 62 | 64 |

*No data taken

HARMONIC OF INTEREST: TENTH

| AMPLITUDE (dB) / SAMPLING PERIOD (nsec) \ TRACK TIME | 3 nsec | 5 nsec | 7 nsec | 9 nsec | 11 nsec | 13 nsec | 15 nsec | 17 nsec |
|---|---|---|---|---|---|---|---|---|
| 146 | ** | * | * | * | * | * | * | * |
| 227 | ** | * | * | * | * | * | * | * |
| 409 | 65 | * | * | * | * | * | * | * |
| 541 | 59 | 65 | 64 | * | 64 | * | * | * |
| 672 | 62 | 60 | 60 | * | 66 | 68 | * | * |
| 804 | 67 | 58 | 58 | * | 64 | 67 | 70 | 67 |

*No data taken

**No data because amplitude is too small to measure

Distribution List - AFAL-TR-78-160

Addresses have been selected on the basis of interest in integrated circuit technology and new developments in the area of A/D converters and sample-and-hold amplifiers. It would be appreciated if recipients would notify AFAL/DHE, W-PAFB, OH of any corrections which should be made to this distribution list.

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